

# LUCID SDR

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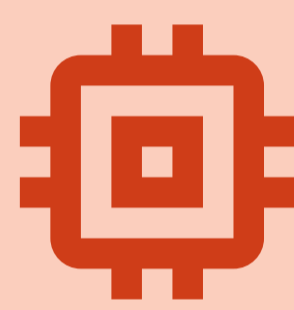
**Lucid SDR is a real-time processing engine for RF signals in frequency ranges between 75 MHz to 6 GHz with 168 MHz bandwidth. Lucid SDR is equipped with an efficiently integrated FPGA based on a Zynq family chip. Our SDR is integrated with three ultra-fast RF transceivers. B4 Limits full product range consists of stable multiphase power supply, multiple communication interfaces, fast RAM, flash memory and full duplex RF input and output paths.**



75(RX)-6000 MHz  
47(TX)-6000 MHz



3x RX RF inputs  
3x TX RF outputs  
in the range up to 6 GHz each



Dual ARM Cortex-A9  
@800MHz Zynq-7030 FPGA SoC  
with 125 K logic cells

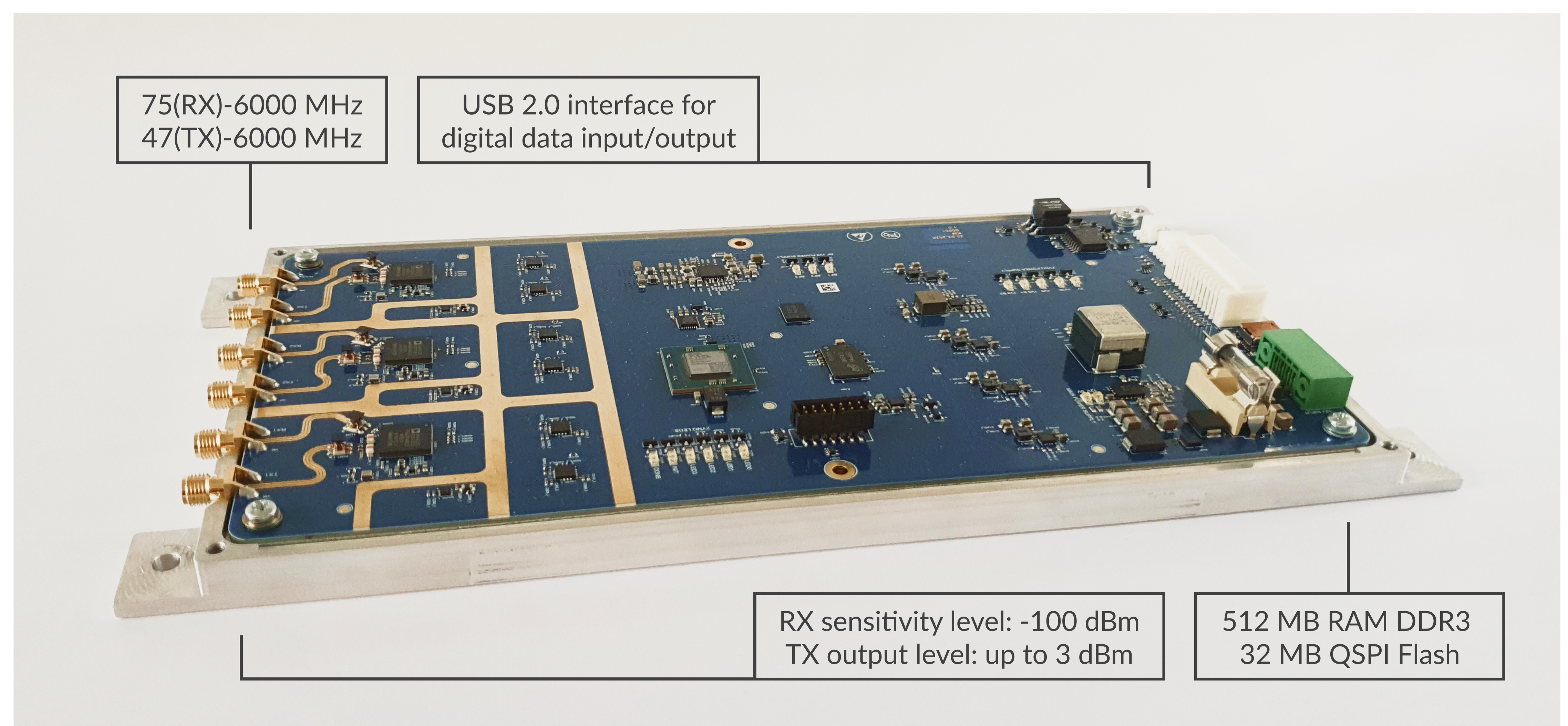


Bandwidth: 168 MHz  
(3x56 MHz)

## ABOUT B4 LIMITS

B4 Limits highly qualified and experienced PhD level team created our **signal processing SDR platform** offering **full flexibility** of use. Our platform can be applied for solutions ranging from **vector signal generator, BTS, spectrum analyzer, jamming and repeater applications** to **uplink activity detection/decoding**.

B4 Limits team also developed **state of the art solutions** around our base product: **Software Defined Radio Platform**. The entire range of products consists of mainly support devices: **power amplifier controller, smart system controller** and the heart of the system **B4 Limits produced SDR**.





# SHORT SPECIFICATION

POWER	FEATURES
Supply voltage: <b>12 V</b>	GNU <b>Radio sink</b> and <b>source blocks</b>
Maximum current consumption: <b>4 A</b>	Libiio, a C, C++, C#, and Python <b>API</b>
Digital signals of voltage levels <b>1.8 V</b>	
PHYSICAL	APPLICATIONS
Operating temperature: <b>-30 to 85 °C</b>	Vector <b>signal generator</b>
PCB dimensions (L x W): <b>235 x 120 mm</b>	<b>Spectrum analyzer</b>
Housing dimensions (L x W x H): <b>245 x 130 x 40 mm</b>	<b>Uplink activity detection/decoding</b> (2G/3G/4G/5G, UHF/VHF, WiFi 2.4/5.0)
PCB weight: <b>0.5 kg</b>	<b>Jamming and repeater applications</b>
Optional aluminium housing weight: <b>1.0 kg</b>	<b>BTS</b>
RF PERFORMANCE	DIGITAL SPECIFICATION
RX/TX isolation level: <b>50 dBm</b>	<b>Dual ARM Cortex-A9 @800 MHz</b>
RX sensitivity level: <b>- 100 dBm</b>	<b>Zynq-7030 FPGA SoC with 125 K logic cells</b>
RX to TX response time: <b>36 µs</b>	<b>3 communication interfaces:</b> CAN, USB, UART
TX output level <b>up to 3 dBm</b>	RAM: <b>512 MB</b>
CONVERSION PERFORMANCE	CUSTOMISATION
Processing speed: <b>6 Gb/s</b>	<b>Customised projects upon request</b>
Sampling speed: <b>61.22 MS/s</b>	On your own <b>via GNU platform</b>
<b>18</b> configurable <b>digital IOs</b> (4 PS, 14 PL)	With <b>B4 Limits</b>

## LUCID SDR VERSIONS

**V1** – equipped with 1 transceiver

**V2** – equipped with 2 transceivers

**V3** – equipped with 3 transceivers

LUCID SDR

