

### Device Features

- 6-bit Serial & Parallel Interface
- 31.5 dB Control Range 0.5 dB step
- Support addressable Function (Addr0-Addr7)
- Glitch-safe attenuation state transitions
- 2.7 V to 5.5 V supply
- 1.8 V or 3.3 V control logic
- Excellent Attenuation Accuracy  
Any bit Attenuation Error <math>\lt; \pm 0.5 \text{ dB}</math> up to 6GHz
- Low Insertion Loss
  - 0.6 dB @ 1GHz
  - 0.8 dB @ 2GHz
  - 1.0 dB @ 3GHz
  - 1.4 dB @ 4GHz
  - 2.1 dB @ 5GHz
- Ultra linearity IIP3 > +63dBm @ 3.5GHz, ATT=0dB
- Input 0.1dB Compression (IP0.1dB) 29dBm @ 3.5GHz, ATT=0dB
- Programming modes
  - Direct parallel
  - Latched parallel
  - Serial Addressable
- Stable Integral Non-Linearity over temperature
- Low Current Consumption 200  $\mu\text{A}$  typical
- -40 °C to +105 °C operating temperature
- ESD rating : Class1C (1KV HBM)
- Lead-free/RoHS2-compliant 24-lead 4mm x 4mm x 0.9mm QFN SMT package



24-lead 4mm x 4 mm x 0.9mm QFN

Figure 1. Package Type

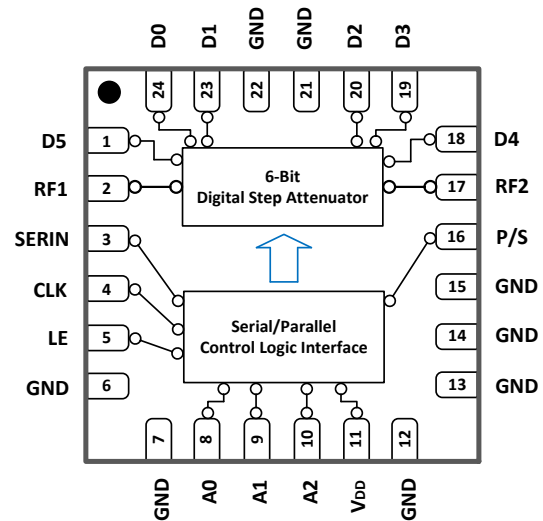


Figure 2. Functional Block Diagram

### Product Description

The BDA4630 is a broadband, Highly accurate 50 $\Omega$  digital step attenuator model which provides adjustable attenuation from 0 to 31.5 dB in 0.5 dB steps. The control interface supports a 6-bit serial interface with 3-bit addressable function and latched parallel interface.

BDA4630 supports a broad operating frequency range from 1MHz to 6.0 GHz. BDA4630 is offering the High linearity, low power consumption, low insertion loss, high attenuation accuracy and low insertion loss less than 2.1dB typical at all frequency band.

The device features a safe state transitions with no negative/positive Glitch technology optimized for excellent step accuracy.

The RF input and output are internally matched to 50  $\Omega$  and do not require any external matching components. The design is bi-directional; therefore, the RF input and output are interchangeable. BDA4630 also features an external negative supply option.

This DSA does not require blocking capacitors. If DC is presented at the RF port, add a blocking capacitor. It is packaged in a RoHS2-compliant with QFN surface mount package.

### Application

- 5G/4G+/4G/3G Cellular Base station/Repeater Infrastructure
- Digital Pre-Distortion
- Distributed Antenna Systems, DAS
- Remote Radio Heads
- NFC Infrastructure
- Test Equipment and sensors
- Military Wireless system
- Cable Infrastructure
- General purpose Wireless

Table 1. Electrical Specifications<sup>1</sup>

Parameter	Condition	Frequency	Min	Typ	Max	Unit
Operating Frequency Range			1		6000	MHz
Attenuation range	0.5dB step			0 - 31.5		dB
Insertion Loss <sup>2</sup>	ATT = 0dB	1MHz - 1GHz		0.5	0.6	dB
	ATT = 0dB	> 1 - 2.2GHz		0.8	0.9	dB
	ATT = 0dB	> 2.2 - 3GHz		1.0	1.0	dB
	ATT = 0dB	> 3 - 4GHz		1.2	1.4	dB
	ATT = 0dB	> 4 - 6GHz		2.1	2.7	dB
Attenuation Error	0-31.5dB	1MHz - 1GHz			±(0.10 + 1.0% of attenuation state)	dB
		> 1 - 2.2GHz			±(0.15 + 1.5% of attenuation state)	dB
		> 2.2 - 3GHz			±(0.15 + 2.5% of attenuation state)	dB
		> 3 - 4GHz			±(0.25 + 3.5% of attenuation state)	dB
		> 4 - 6GHz			±(0.25 + 5.0% of attenuation state)	dB
Input Return Loss	ATT = 0dB	1 - 4GHz		21		dB
		> 4 - 6GHz		9		
Output Return Loss	ATT = 0dB	1 - 4GHz		21		dB
		> 4 - 6GHz		9		
Relative Phase Error	All states	1GHz		7		degree
		2GHz		15		
		3GHz		23		
		4GHz		31		
		5GHz		39		
		6GHz		44		
Input Linearity	Input 0.1dB Compression point	ATT = 0dB	3.5GHz	29		dBm
		Pin = +18dBm/tone, Δf = 10kHz ATT = 0.0dB RF Input = RF1 Port	2.5GHz	53		dBm
	3.5GHz		64			
	4.5GHz		56			
	Pin = +18dBm/tone, Δf = 10kHz ATT = 31.5dB RF Input = RF1 Port	2.5GHz	57		dBm	
		3.5GHz	54			
		4.5GHz	54			
	Pin = +18dBm/tone, Δf = 10kHz ATT = 0.0dB RF Input = RF2 Port	2.5GHz	62		dBm	
		3.5GHz	64			
		4.5GHz	58			
Pin = +18dBm/tone, Δf = 10kHz ATT = 31.5dB RF Input = RF2 Port	2.5GHz	50		dBm		
	3.5GHz	58				
	4.5GHz	54				
RF Rising / Falling Time	10%/90% RF	2GHz		95		ns
Switching time	50% CTRL to 90% or 10% RF	2GHz		210		ns
Settling time	50% CTRL to Max or Min Attenuation to settle within 0.05 dB of final value	2GHz		500		ns
Attenuation transient(envelope) <sup>3</sup>	Positive Glitch, Any ATT step			0.3		dB
Maximum Spurious level on any RF port <sup>4</sup>	Measured at RF ports	< 7MHz		< -145		dBm

1. Device performance is measured on a BeRex Evaluation board Kit at 25°C, 50 Ω system, VDD=+3.3V

2. The Evaluation board Kit insertion loss (PCB & RF Connector) is de-embedded.

3. Attenuation Transient is glitch level due to attenuation transitions

4. The unwanted spurious due to built-in negative voltage generator. Typical generated fundamental frequency is 6.8MHz.

**Table 2. Recommended operating Condition**

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage	$V_{DD}$		2.7		5.5	V
Supply Current	$I_{DD}$			200	310	$\mu$ A
Digital Control Input	High	$V_{CTLH}$	$V_{DD}=3.3V$ or $5V$	1.17	3.6	V
	Low	$V_{CTLL}$	$V_{DD}=3.3V$ or $5V$	-0.3	0.6	V
Operating Temperature Range	$T_{Case}$	Exposed Paddle	-40		105	$^{\circ}$ C
RF Max Input Power	$P_{IN\_CW}$	RF1 or RF2, CW			23	dBm
Impedance	$Z_{Load}$	Single ended		50		$\Omega$

Specifications are not guaranteed over all recommended operating conditions.

**Table 3. Absolute Maximum Ratings**

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	$V_{DD}$	-0.3		5.5	V
Digital input voltage	$V_{CTL}$	-0.3		3.6	V
Maximum input power	$P_{IN\_CWMAX}$			34	dBm
Temperature	Storage	$T_{ST}$	-65	150	$^{\circ}$ C
	Reflow	$T_R$		260	$^{\circ}$ C
ESD Sensitivity	HBM <sup>1</sup>	$ESD_{HBM}$		1000 (Class 1C)	V
	CDM <sup>2</sup>	$ESD_{CDM}$		1000 (Class C4)	V

Operation of this device above any of these parameters may result in permanent damage.

1. HBM : Human Body Model (JEDEC Standard JS-001-2017)

2. CDM : Charged Device Model (JEDEC Standard J-STD-020)

Figure 3. Pin Configuration (Top View)

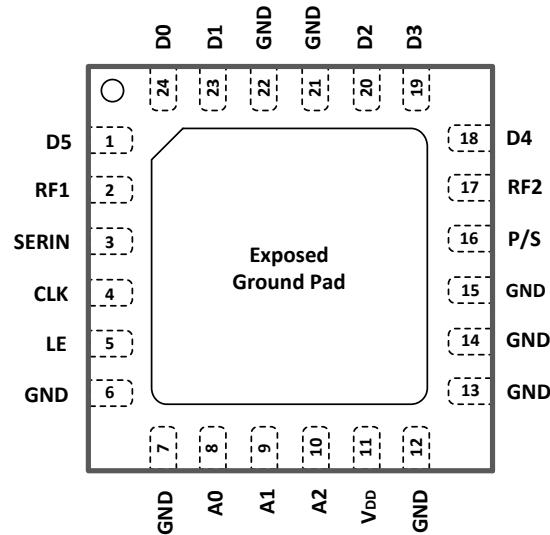


Table 4. Pin Description

Pin	Pin name	Description
1	D5 <sup>2</sup>	Attenuation control bit, 16dB
2	RF1 <sup>1</sup>	RF1 port (Attenuator RF Input) This pin can also be used as an output because the design is bi-directional. RF1 is dc-coupled and matched to 50 Ω.
3	SERIN	Serial interface data input
4	CLK	Serial interface clock input
5	LE	Latch Enable input
6, 7, 12, 13, 14, 15, 21, 22	Ground	Ground, These pins must be connected to ground
8	A0	Address bit A0 connection
9	A1	Address bit A1 connection
10	A2	Address bit A2 connection
11	VDD	Power Supply (nominal 3.3V)
16	P/S	Parallel/Serial Mode Select. For parallel mode operation, set this pin to LOW. For serial mode operation, set this pin to HIGH.
17	RF2 <sup>1</sup>	RF2 port (Attenuator RF Output.) This pin can also be used as an input because the design is bi-directional. RF2 is dc-coupled and matched to 50 Ω.
18	D4 <sup>2</sup>	Attenuation control bit, 8dB
19	D3 <sup>2</sup>	Attenuation control bit, 4dB
20	D2 <sup>2</sup>	Attenuation control bit, 2dB
23	D1 <sup>2</sup>	Attenuation control bit, 1dB
24	D0 <sup>2</sup>	Attenuation control bit, 0.5dB
Pad	GND	Exposed pad: The exposed pad must be connected to ground for proper operation

1. RF pins 2 and 17 must be at 0V DC. The RF pins do not require DC blocking capacitors for proper Operation if the 0V DC requirement is met  
 2. Ground D0 - D5 if not in use or serial mode.

### Programming Options

BDA4630 can be programmed using either the parallel or serial interface, which is selectable via P/S pin(Pin13).

Serial mode is selected by pulling it to a voltage logic HIGH and parallel mode is selected by setting P/S to logic LOW.

### Serial Control Mode

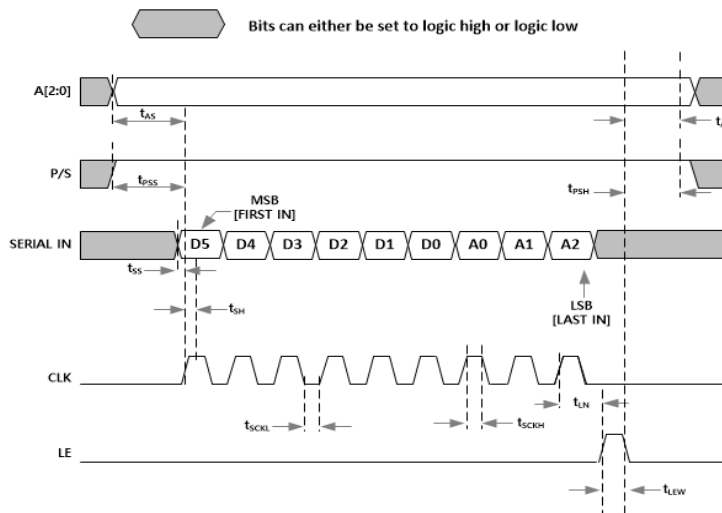
The serial interface is a 6-bit shift register to shift in the data MSB (D5) first. When serial programming is used, It is recommended all the parallel control input pins (1, 18, 19, 20, 23, 24) are grounded.

It is controlled by three CMOS-compatible signals: SERIN, Clock, and Latch Enable (LE).

**Table 5. Truth Table for Serial Control Word**

Digital Control Input						Attenuation state (dB)
D5 (MSB)	D4	D3	D2	D1	D0 (LSB)	
LOW	LOW	LOW	LOW	LOW	LOW	0 (RL)
LOW	LOW	LOW	LOW	LOW	HIGH	0.5
LOW	LOW	LOW	LOW	HIGH	LOW	1
LOW	LOW	LOW	HIGH	LOW	LOW	2
LOW	LOW	HIGH	LOW	LOW	LOW	4
LOW	HIGH	LOW	LOW	LOW	LOW	8
HIGH	LOW	LOW	LOW	LOW	LOW	16
HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	31.5

**Figure 4. Serial Mode Timing Diagram**



BDA4630 Serial mode is selected by pulling it to logic HIGH. The serial interface is a 9-bit shift register made up of two words. The first 6-bit word is the Attenuation word, which controls the DSA state. The second word is the address word, which uses 3 bits that must match the hard wired A0-A2 programming in order to change the DSA state. If no external connections are made to A0 – A2 then internally they will default to 000 due to internal pull down resistors. If these 3 external preset address bits are not matched with the SPI loaded address bits, then the current attenuator state will remain unchanged. This allows up to 8 serial-controlled devices to be used on a single board, which share a common SERIN, CLK and LE.

When serial programming is used, all the parallel control input pins 1, 18, 19, 20, 23, 24 can be left grounded or open.

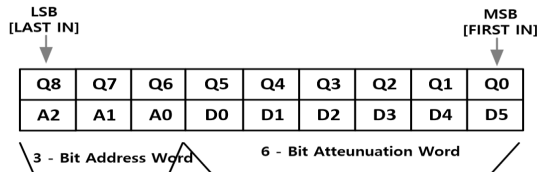
**Table 6. Serial Interface Timing Specifications**

Symbol	Parameter	Min	Typ	Max	Unit
$f_{CLK}$	Serial data clock frequency			10	MHz
$t_{PS}$	Parallel data setup time	100			ns
$t_{PH}$	Parallel data hold time	100			ns
$t_{AS}$	Address setup time	100			ns
$t_{AH}$	Address hold time	100			ns
$t_{PSS}$	Parallel/Serial setup time	100			ns
$t_{PSH}$	Parallel/Serial hold time	100			ns
$t_{SCK}$	Minimum serial period	70			ns
$t_{SS}$	Serial Data setup time	10			ns
$t_{SH}$	Serial Data hold time	10			ns
$t_{LN}$	LE setup time	10			ns
$t_{LEW}$	Minimum LE pulse width	30			ns

### Serial Register Map

The BDA4630 can be programmed via the serial control on the rising edge of Latch Enable (LE) which loads the last 6-bits attenuation word and 3-bits address word in the SHIFT Register. Serial Data is clocked in MSB(D5) first. The shift register must be loaded while LE is kept LOW to prevent changing the attenuation value during data is inputted.

**Figure 5. Serial Register Map**



The serial register consist of 9 bits as shown in Figure 5. First six bits from LSB are Attenuation word, four bits after that are Address word. The Attenuation word is DSA attenuation control bit and the Address word is static logical bit determined by A0, A1 and A2 digital inputs. The attenuation word is derived directly from the value of the attenuation state. To find the attenuation word, multiply the value of the state by two because of 0.5dB step up to 31.5dB ( total 63 Attenuation state), then convert to binary.

For example, to program attenuation 15.5dB state of addr[5] BDA4630 :

Attenuation state $2 \times 15.5 = 31$ $31 \rightarrow 011111$ $D5-D0 : 111110$	Address state Digital input of A2,A1,A0 pin = 101
--	--

Serial Input : 101111110

1	0	1	1	1	1	1	1	0
A2	A1	A0	D0	D1	D2	D3	D4	D5

**Table 7. Truth Table for 3bit Address Word**

Address Digital Control Input			Address Setting	Addr No.
A2 (LSB)	A1	A0 (MSB)		
LOW	LOW	LOW	000	Addr[0]
LOW	LOW	HIGH	001	Addr[1]
LOW	HIGH	LOW	010	Addr[2]
LOW	HIGH	HIGH	011	Addr[3]
HIGH	LOW	LOW	100	Addr[4]
HIGH	LOW	HIGH	101	Addr[5]
HIGH	HIGH	LOW	110	Addr[6]
HIGH	HIGH	HIGH	111	Addr[7]

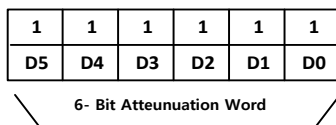
**Table 8. Mode Selection**

P/S	Control Mode
LOW	Parallel
HIGH	Serial

### Power-UP states Settings

The BDA4630 will always initialize to the maximum attenuation setting (31.5 dB) on power-up for both the Serial and Latched Parallel modes of operation and will remain in this setting until the user latches in the next programming word. In Direct Parallel mode, the DSA can be preset to any state within the 31.5 dB range by pre-setting the Parallel control pins prior to power-up. In this mode, there is a 400 μs delay between the time the DSA is powered-up to the time the desired state is set.

**Figure 6. Default Attenuation word for Power-up state**



### Programming Options

#### Parallel Control Mode

The parallel control interface has seven digital control input lines (D5 to D0) to set the attenuation value. D5 is the most significant bit (MSB) that selects the 16 dB attenuator stage, and D0 is the least significant bit (LSB) that selects the 0.5 dB attenuator stage.

#### Direct Parallel Mode

For direct parallel mode, The LE pin must be kept HIGH. The attenuation state is changed by the control voltage inputs (D0 to D5) directly. This mode is ideal for manual control of the attenuator. In this mode the device will immediately react to any voltage changes to the parallel control pins [pins 1, 18, 19, 20, 23, 24]. Use direct parallel mode for the fastest settling time.

#### Latched Parallel Mode

The LE pin must be kept LOW when changing the control voltage inputs (D0 to D5) to set the attenuation state. When the desired state is set, LE must be toggled HIGH to transfer the 6-bit data to the bypass switches of the attenuator array, and then toggled LOW to latch the change into the device until the next desired attenuation change (see Figure 7 and Table 9).

- Set P/S is logic LOW.
- Set LE to logic LOW.
- Adjust pins [1, 18, 19, 20, 23, 24] to the desired attenuation setting. (Note the device will not react to these pins while LE is a logic LOW).
- Pull LE to a logic HIGH. The device will then transition to the attenuation settings reflected by pins D5 - D0.
- If LE is pulled to a logic LOW then the attenuator will not change state.

Latched Parallel Mode implies a default state for when the device is first powered up with P/S pin set for logic LOW and LE logic LOW. In this case the default setting is Maximum attenuation.

### Switching Feature Description

#### Glitch-Safe Attenuation State Transient

The BDA4630 is the latest product applied *Glitch-Safe* technology with less than 1dB ringing (pos/neg) across the attenuation range when changing attenuation states. This technology protects Amplifiers or ADC during transitions between attenuation states. (see Figure 32,33).

Table 9. Truth Table for the Parallel Control Word

D5	D4	D3	D2	D1	D0	P/S	LE	Attenuation State(dB)
LOW	LOW	LOW	LOW	LOW	LOW	LOW	HIGH	0 (RL)
LOW	LOW	LOW	LOW	LOW	HIGH	LOW	HIGH	0.5
LOW	LOW	LOW	LOW	HIGH	LOW	LOW	HIGH	1.0
LOW	LOW	LOW	HIGH	LOW	LOW	LOW	HIGH	2.0
LOW	LOW	HIGH	LOW	LOW	LOW	LOW	HIGH	4.0
LOW	HIGH	LOW	LOW	LOW	LOW	LOW	HIGH	8.0
HIGH	LOW	LOW	LOW	LOW	LOW	LOW	HIGH	16.0
HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	LOW	HIGH	31.5

Figure 7. Latched Parallel Mode Timing Diagram

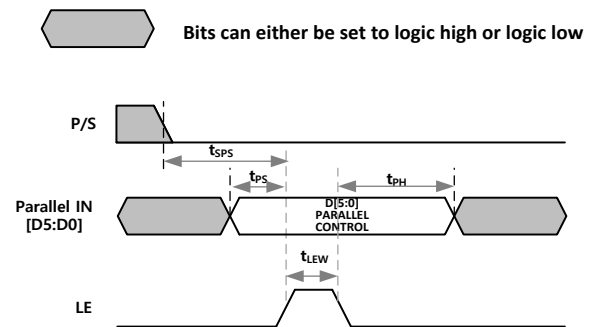


Table 10. Parallel Interface Timing Specifications

Symbol	Parameter	Min	Typ	Max	Unit
$t_{SPS}$	Serial to Parallel Mode Setup Time	100			ns
$t_{LEW}$	Minimum LE pulse width	10			ns
$t_{PH}$	Data hold time from LE	10			ns
$t_{PS}$	Data setup time to LE	10			ns

#### Typical RF Performance Plot - BDA4630 EVK - PCB

Typical Performance Data @ 25°C and  $V_{DD} = 3.3V$ , EVKit RF connector and board losses are de-embedded, unless otherwise noted

Figure 8. Insertion loss vs Temperature

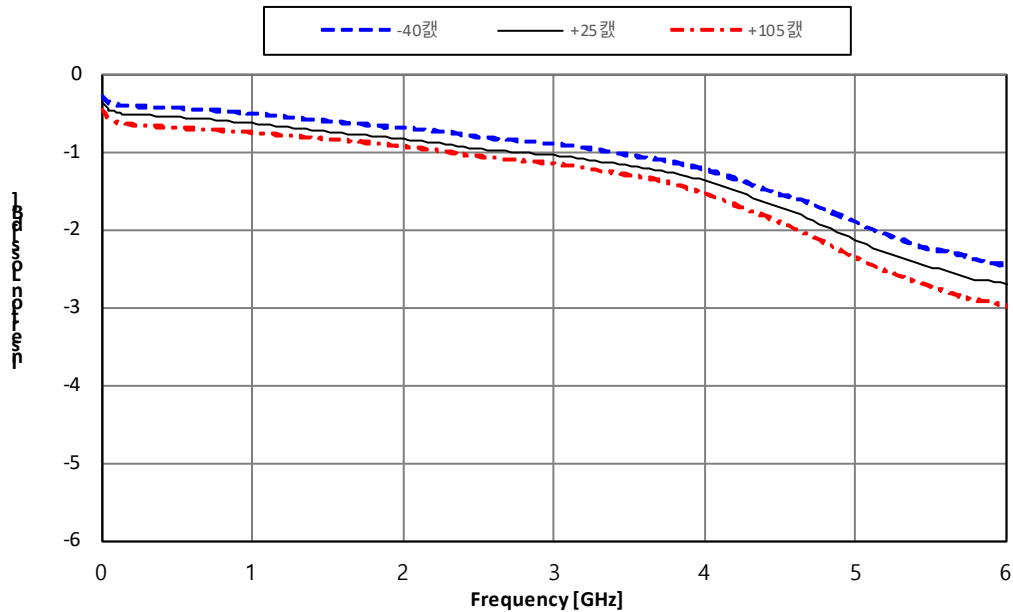
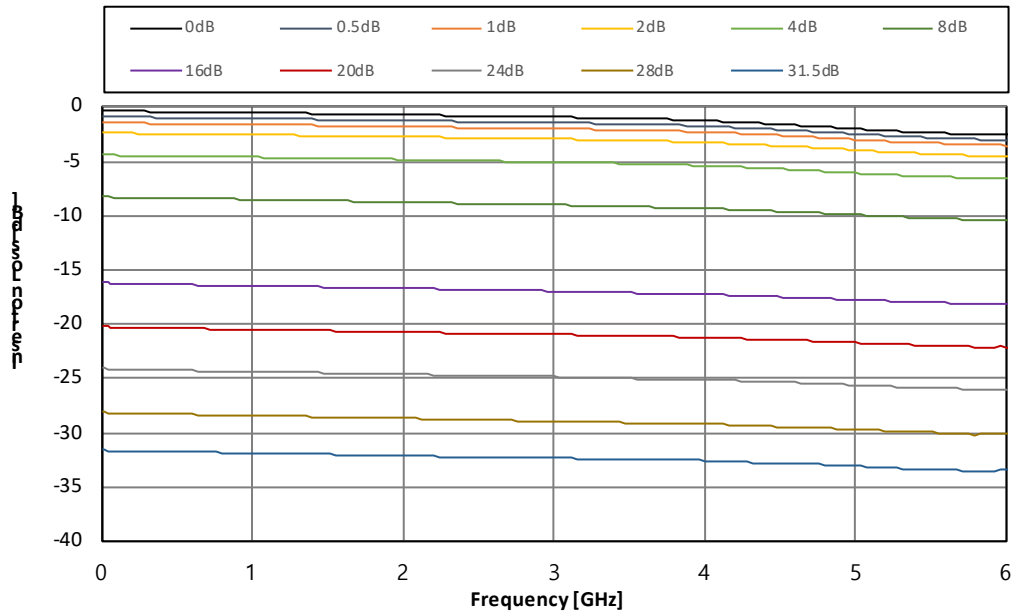


Figure 9. Insertion loss vs Attenuation Setting





### Typical RF Performance Plot - BDA4630 EVK - PCB

Typical Performance Data @ 25°C and  $V_{DD} = 3.3V$ , EVKit RF connector and board losses are de-embedded, unless otherwise noted

Figure 10. Input Return Loss vs Attenuation Setting

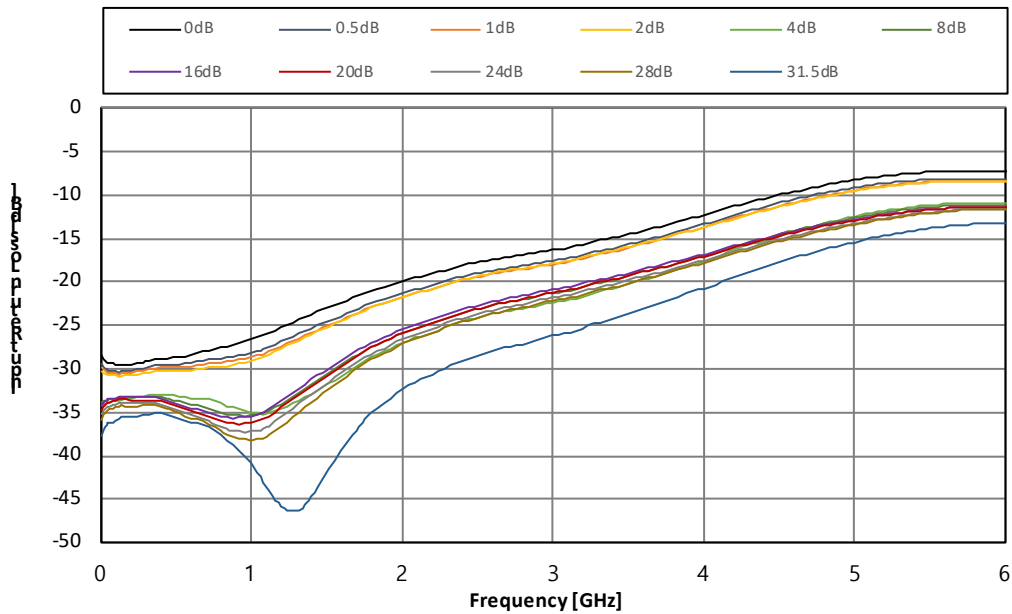
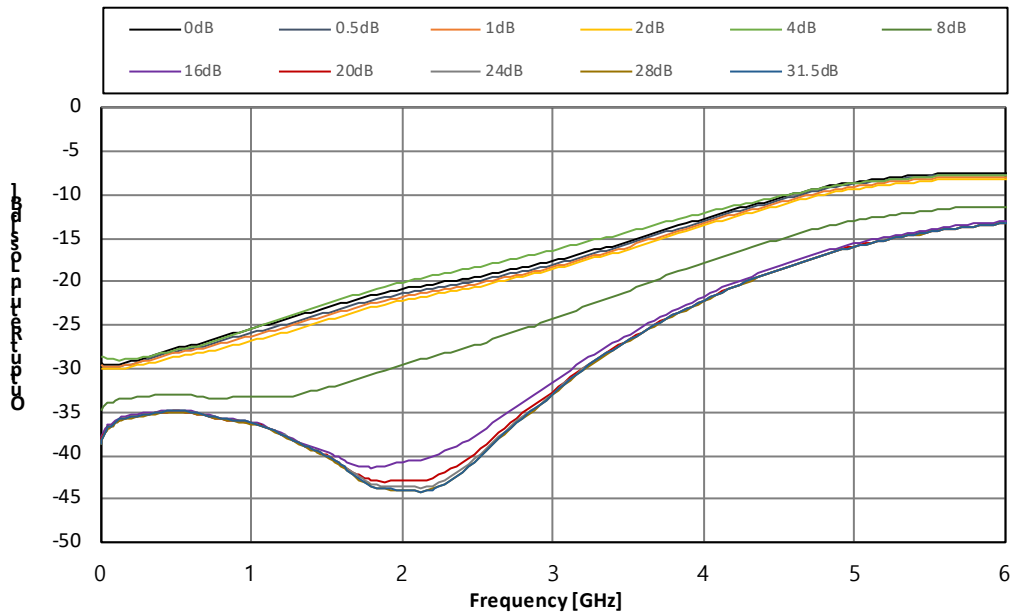


Figure 11. Output Return Loss vs Attenuation Setting



### Typical RF Performance Plot - BDA4630 EVK - PCB

Typical Performance Data @ 25°C and  $V_{DD} = 3.3V$ , EVKit RF connector and board losses are de-embedded, unless otherwise noted

Figure 12. Input Return Loss for 16dB Attenuation Setting vs Temperature

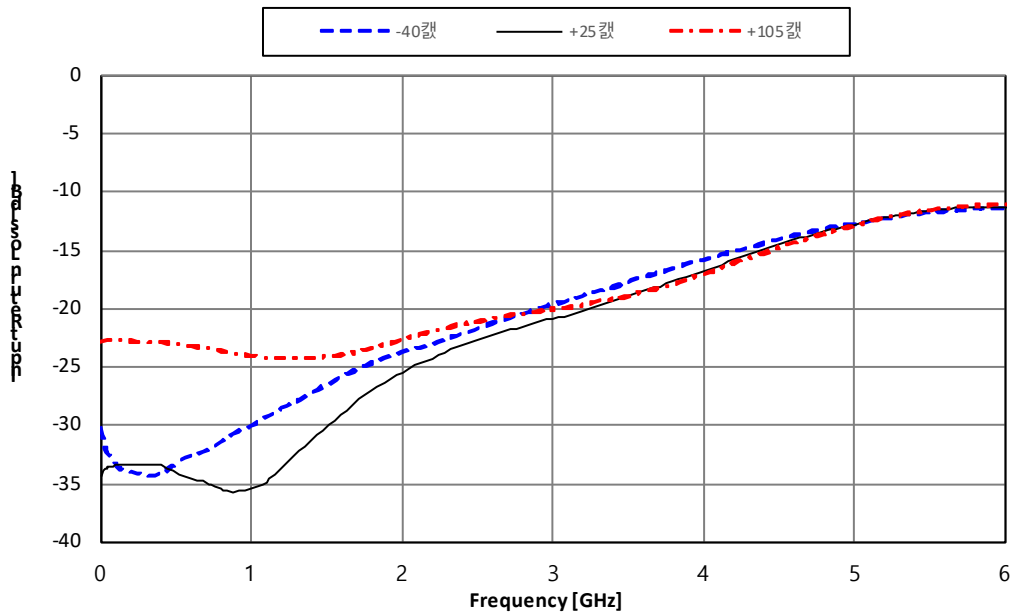
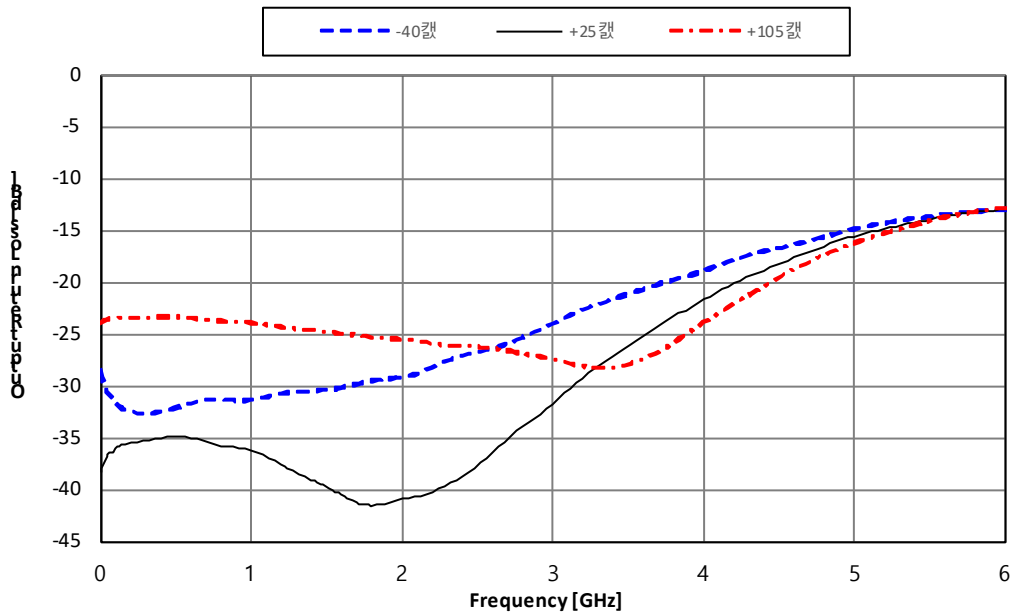
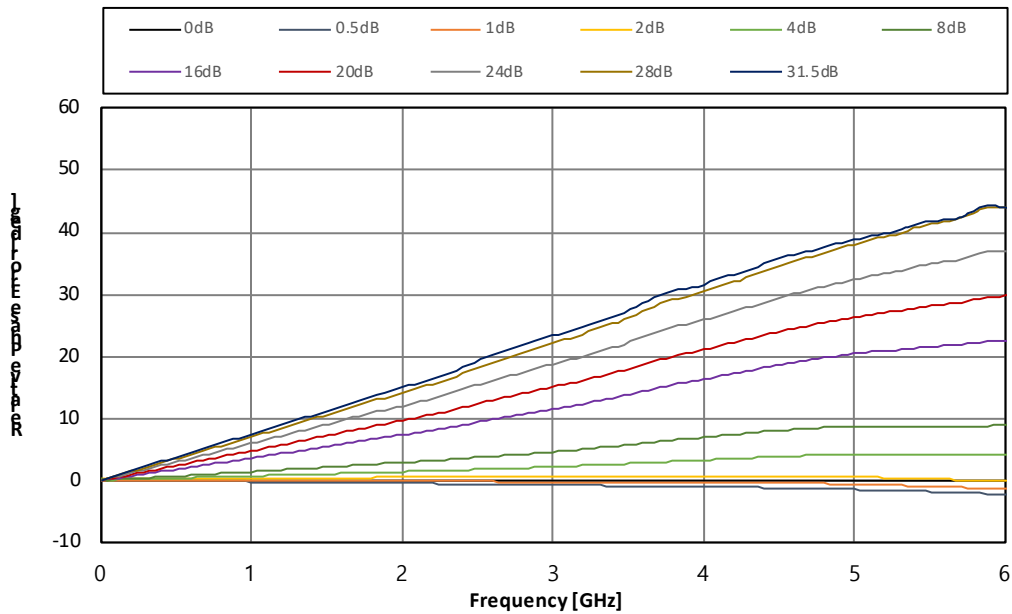
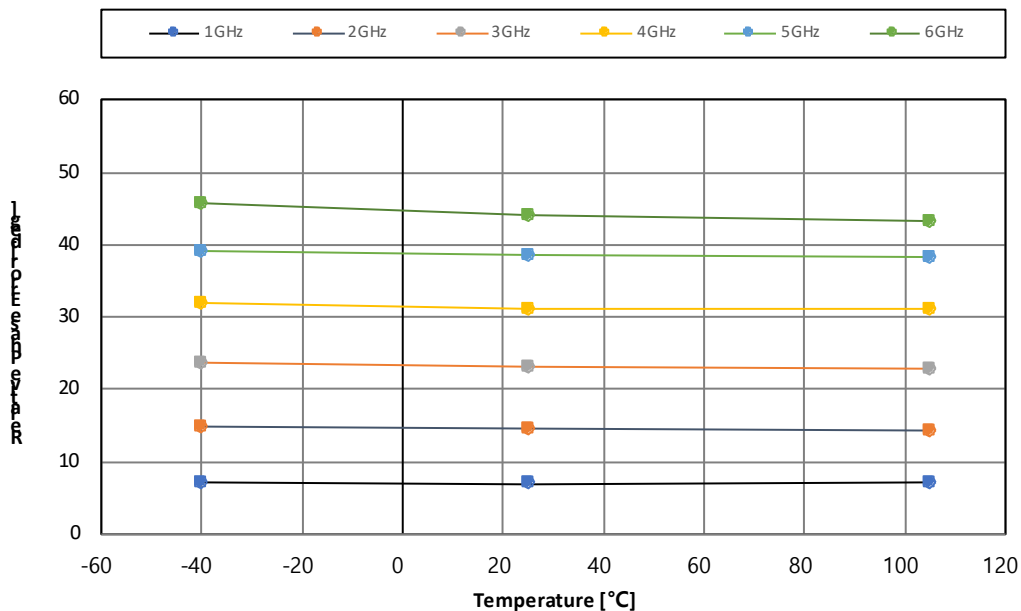


Figure 13. Output Return Loss for 16dB Attenuation Setting vs Temperature



**Typical RF Performance Plot - BDA4630 EVK - PCB**

 Typical Performance Data @ 25°C and  $V_{DD} = 3.3V$ , EVKit RF connector and board losses are de-embedded, unless otherwise noted

**Figure 14. Relative Phase Error vs Attenuation Setting**

**Figure 15. Relative Phase Error for 31.5dB Attenuation Setting vs Frequency**


### Typical RF Performance Plot - BDA4630 EVK - PCB

Typical Performance Data @ 25°C and  $V_{DD} = 3.3V$ , EVKit RF connector and board losses are de-embedded, unless otherwise noted

Figure 16. Attenuation Error @900MHz vs Temperature

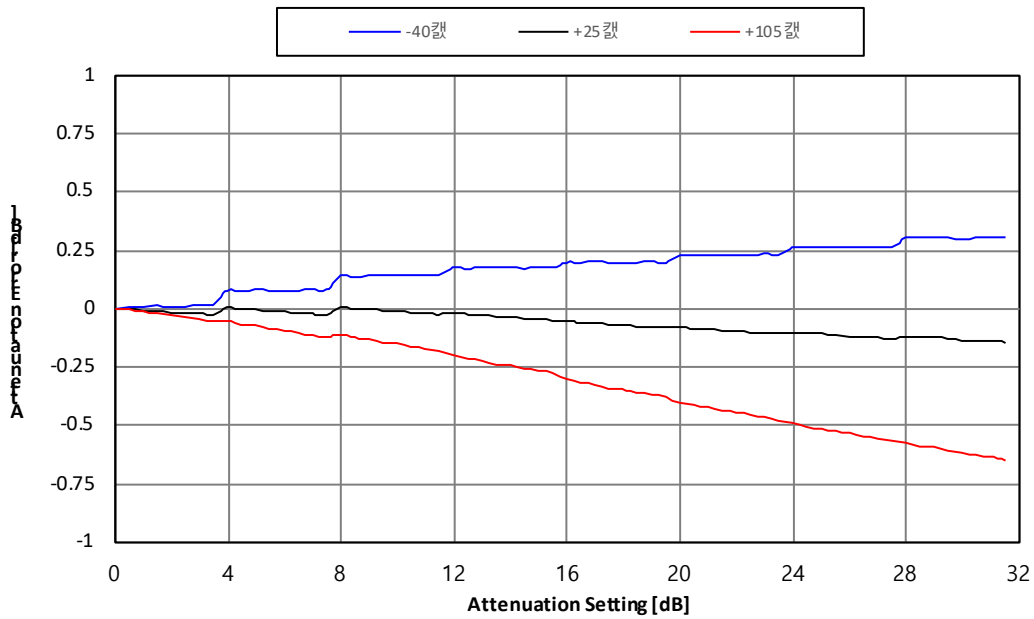
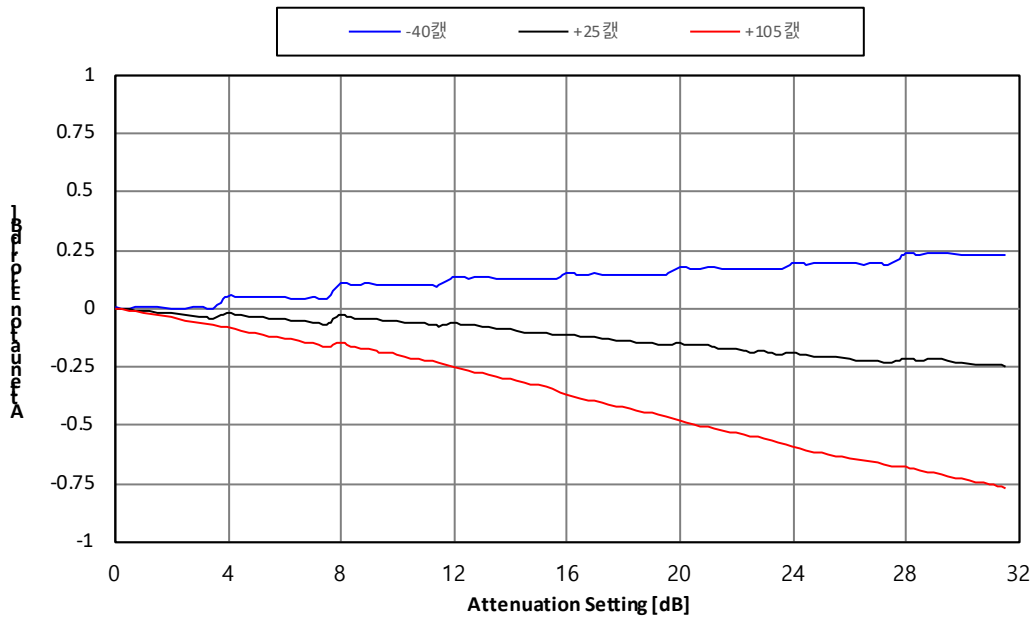


Figure 17. Attenuation Error @1800MHz vs Temperature



### Typical RF Performance Plot - BDA4630 EVK - PCB

Typical Performance Data @ 25°C and  $V_{DD} = 3.3V$ , EVKit RF connector and board losses are de-embedded, unless otherwise noted

Figure 18. Attenuation Error @2200MHz vs Temperature

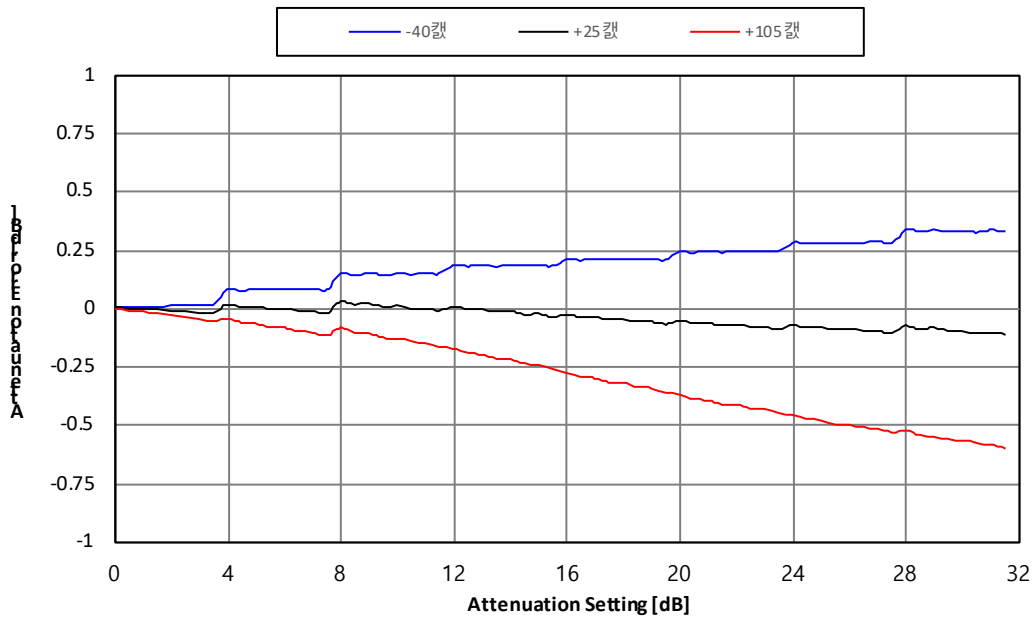
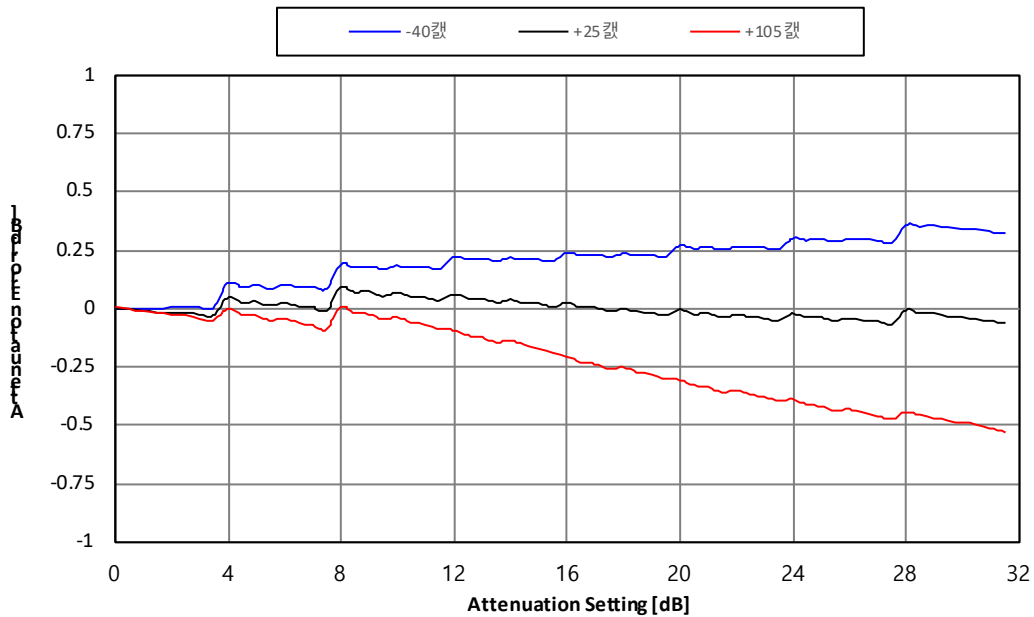


Figure 19. Attenuation Error @3500MHz vs Temperature



### Typical RF Performance Plot - BDA4630 EVK - PCB

Typical Performance Data @ 25°C and  $V_{DD} = 3.3V$ , EVKit RF connector and board losses are de-embedded, unless otherwise noted

Figure 20. Attenuation Error @4600MHz vs Temperature

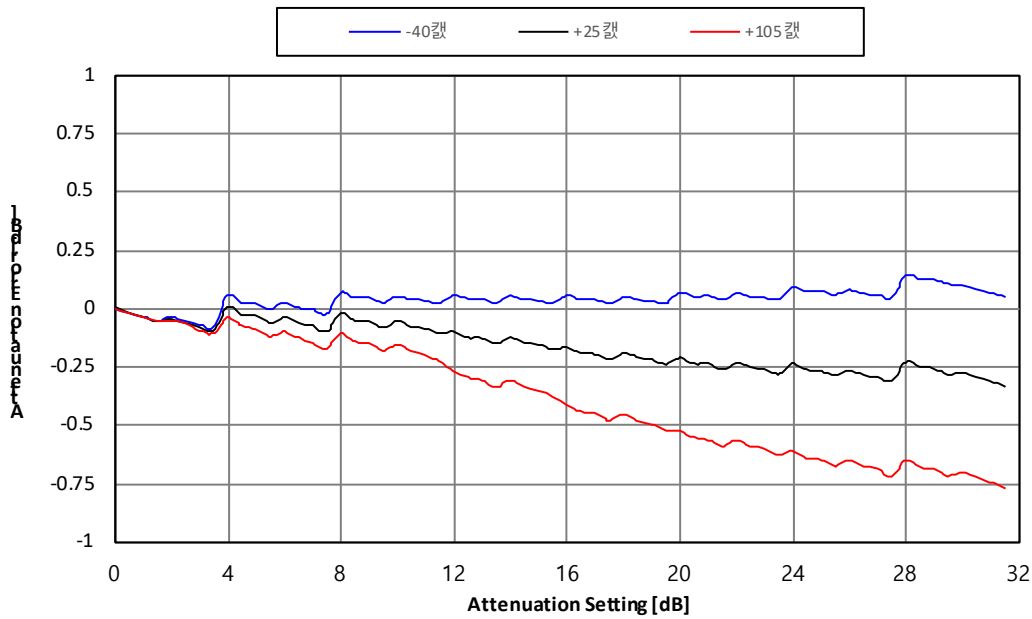
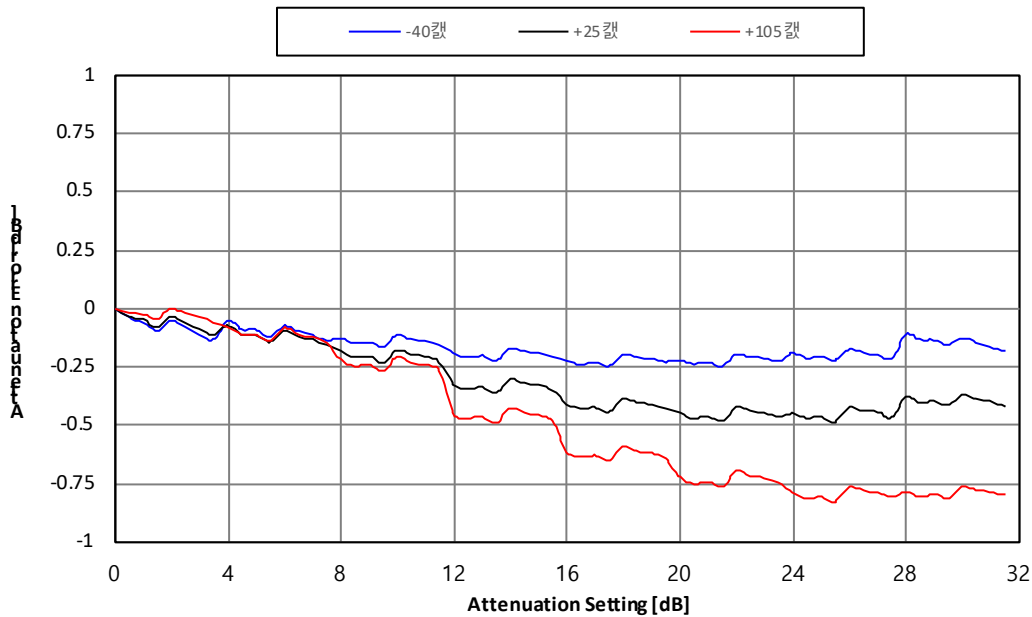


Figure 21. Attenuation Error @5800MHz vs Temperature



### Typical RF Performance Plot - BDA4630 EVK - PCB

Typical Performance Data @ 25°C and  $V_{DD} = 3.3V$ , EVKit RF connector and board losses are de-embedded, unless otherwise noted

Figure 22. IIP3 @ 2500MHz vs Temperature

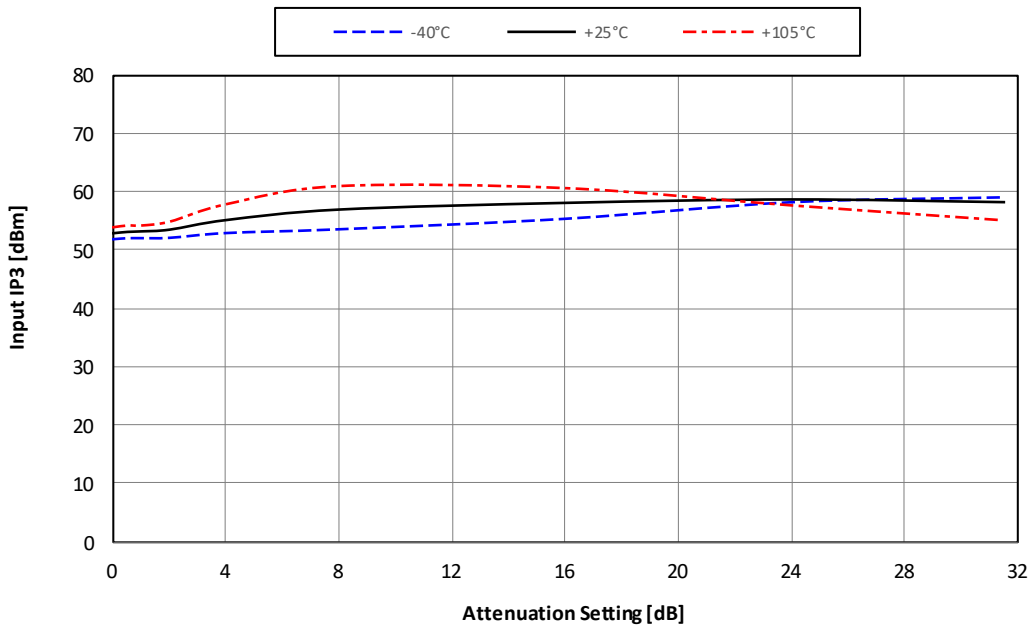
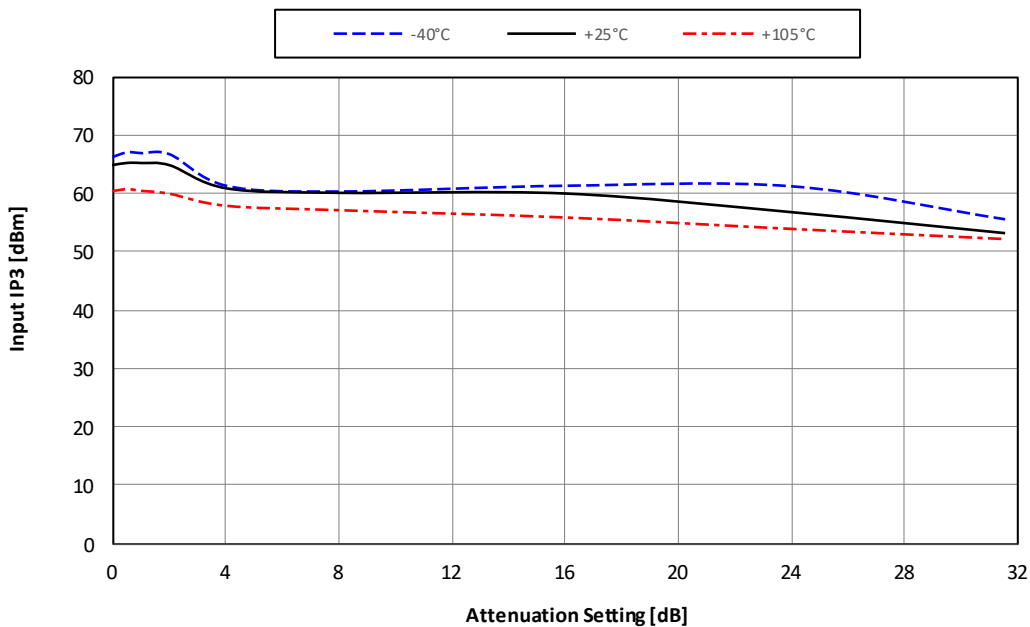


Figure 23. IIP3 @ 3500MHz vs Temperature



### Typical RF Performance Plot - BDA4630 EVK - PCB

Typical Performance Data @ 25°C and  $V_{DD} = 3.3V$ , EVKit RF connector and board losses are de-embedded, unless otherwise noted

Figure 24. IIP3 @ 4500MHz vs Temperature

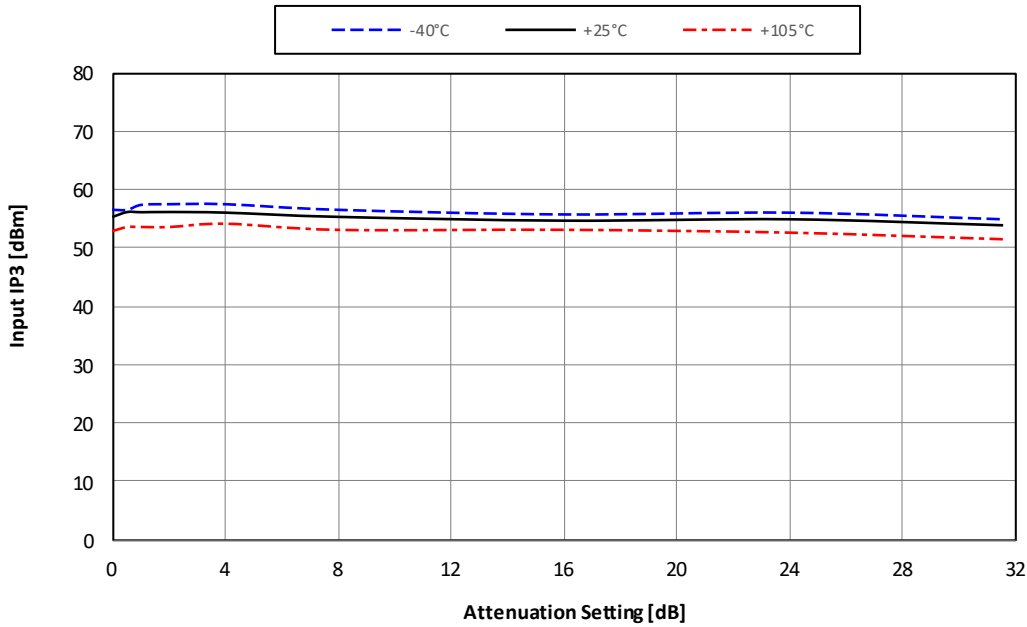
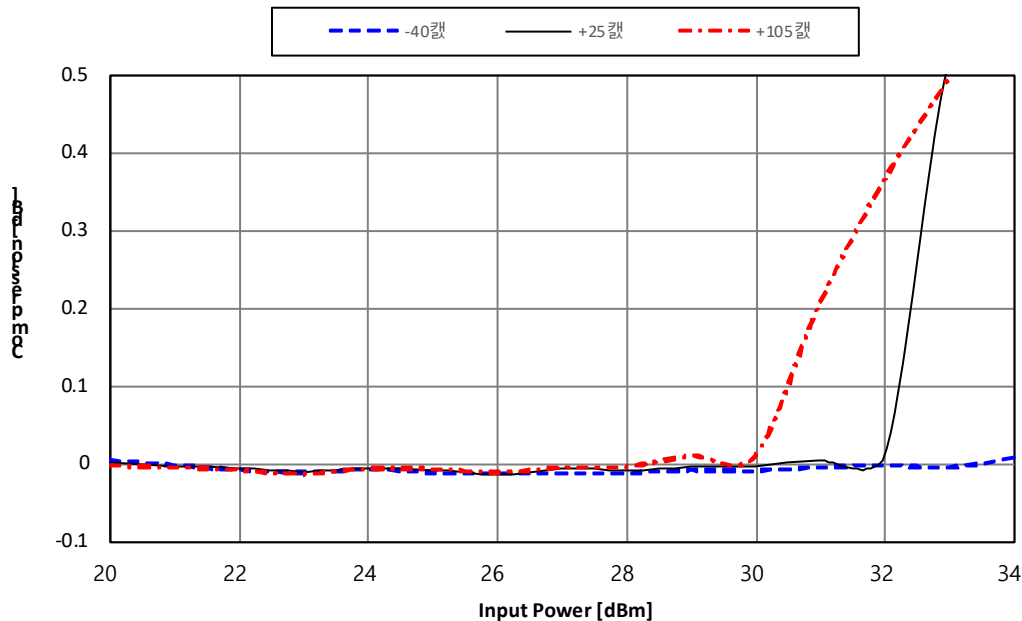


Figure 25. Input 0.1dB Compression @2500MHz vs Temperature





### Typical RF Performance Plot - BDA4630 EVK - PCB

Typical Performance Data @ 25°C and  $V_{DD} = 3.3V$ , EVKit RF connector and board losses are de-embedded, unless otherwise noted

Figure 26. Input 0.1dB Compression @3500MHz vs Temperature

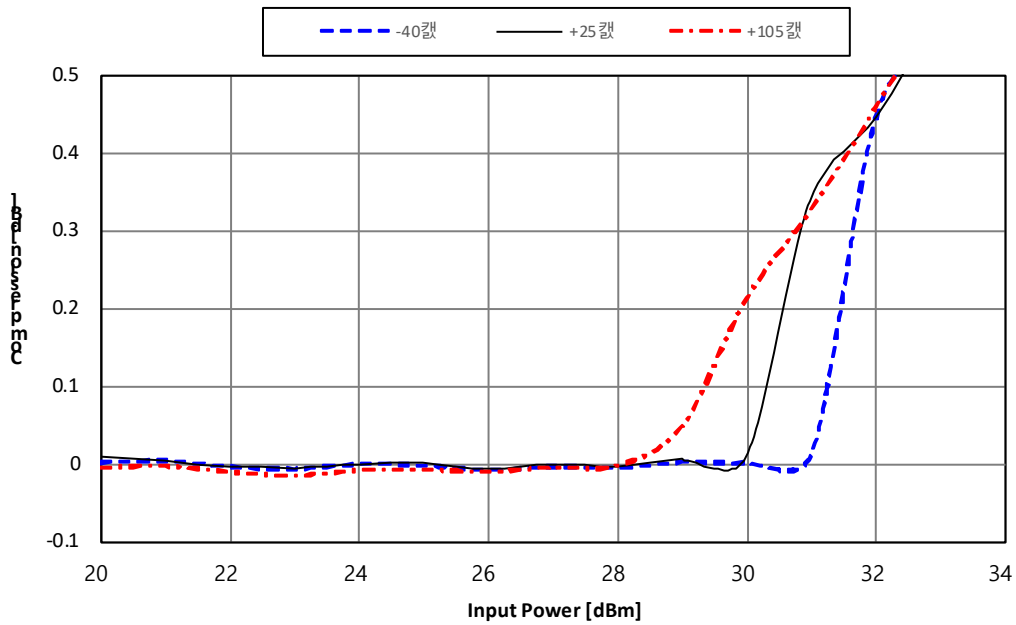
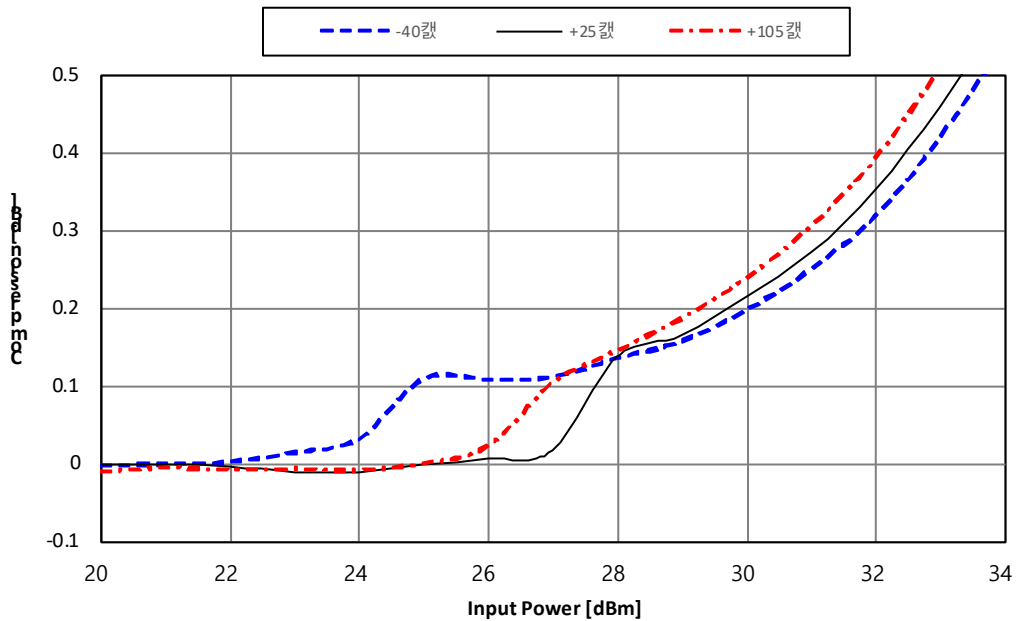
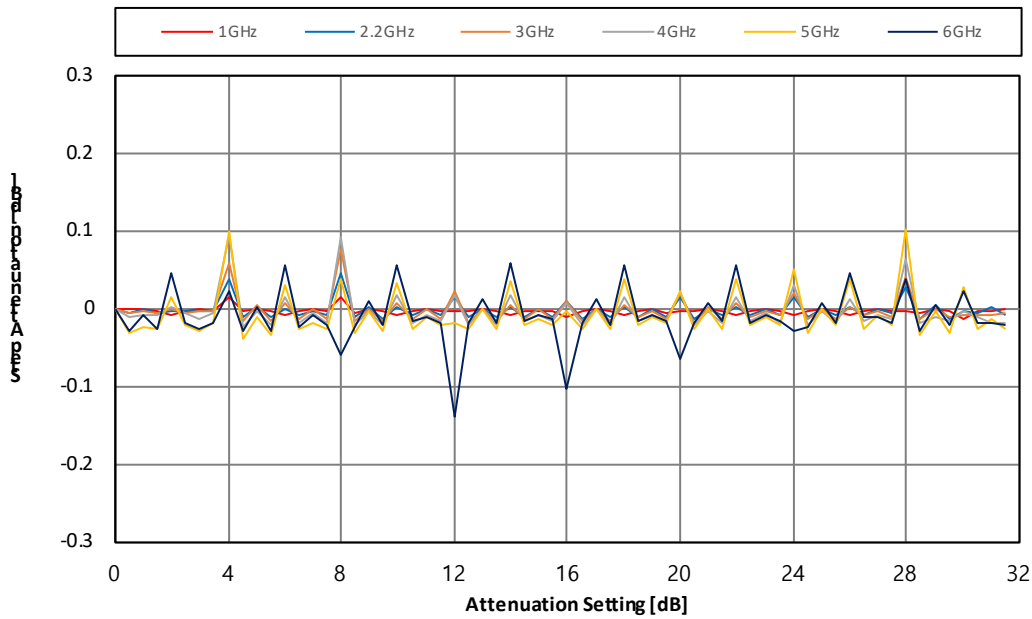
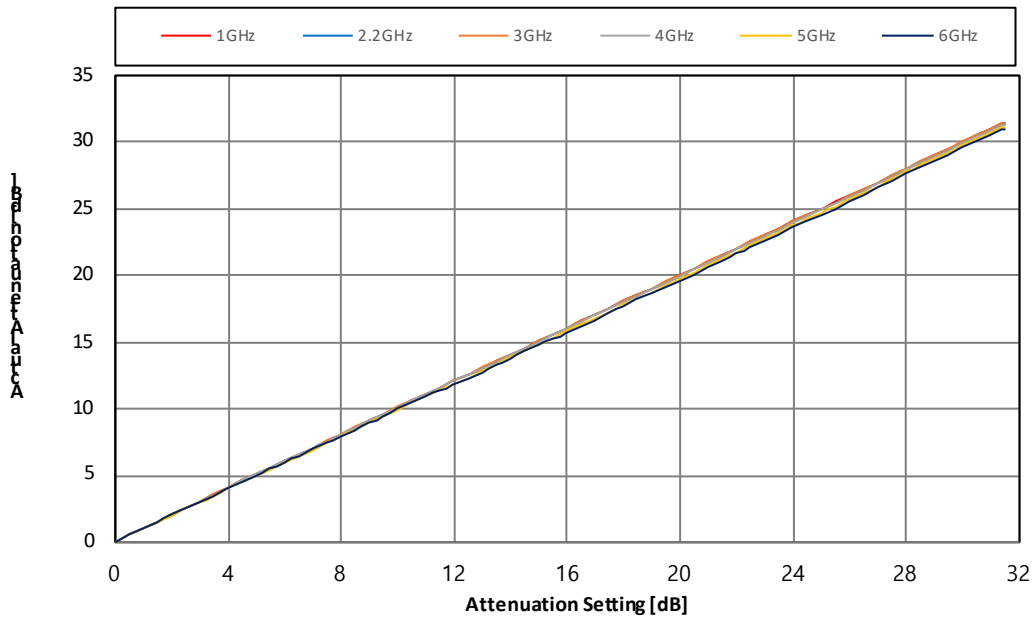


Figure 27. Input 0.1dB Compression @4500MHz vs Temperature



**Typical RF Performance Plot - BDA4630 EVK - PCB**

 Typical Performance Data @ 25°C and  $V_{DD} = 3.3V$ , EVKit RF connector and board losses are de-embedded, unless otherwise noted

**Figure 28. 0.5dB Step Attenuation vs Frequency**

**Figure 29. 0.5dB Step Actual Attenuation vs Frequency**


### Typical RF Performance Plot - BDA4630 EVK - PCB

Typical Performance Data @ 25°C and  $V_{DD} = 3.3V$ , EVKit RF connector and board losses are de-embedded, unless otherwise noted

Figure 30. Major State Bit Error vs Attenuation Setting

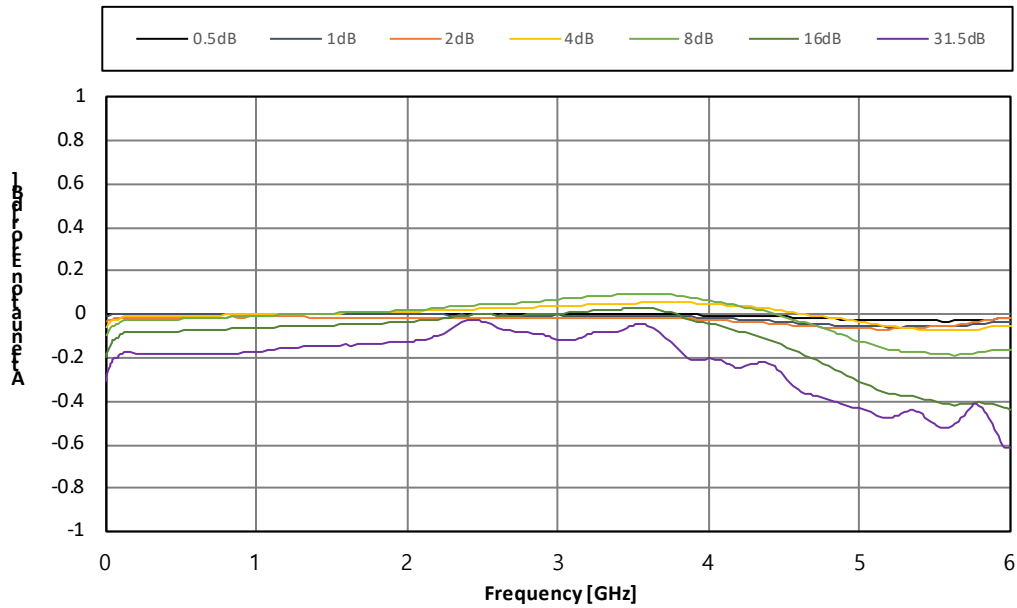
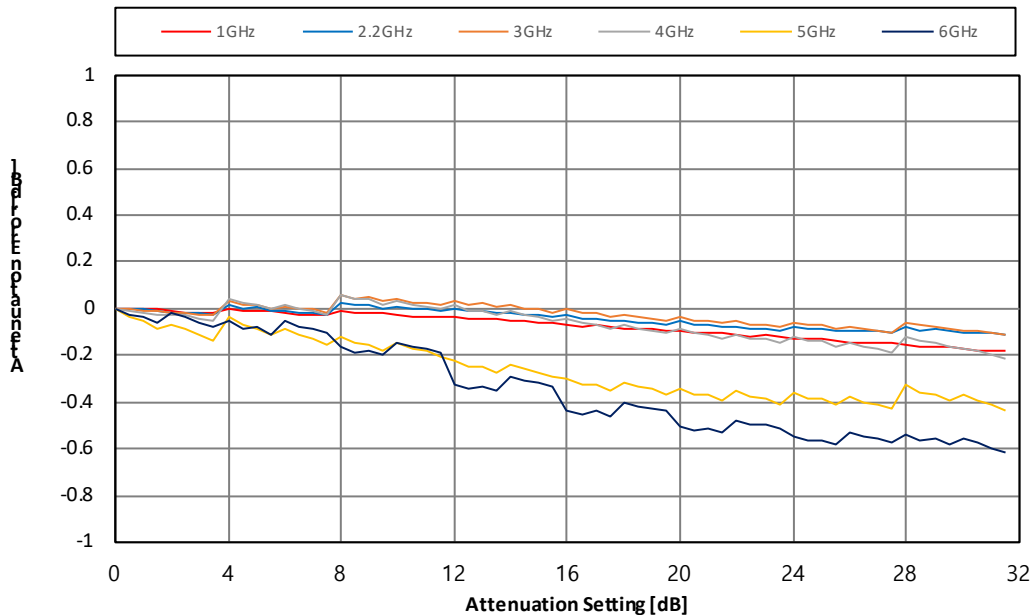


Figure 31. 0.5dB Step Attenuation Error vs Frequency



### Typical RF Performance Plot - BDA4630 EVK - PCB

Typical Performance Data @ 25°C and  $V_{DD} = 3.3V$ , EVKit RF connector and board losses are de-embedded, unless otherwise noted

Figure 32. Attenuation Transient (15.5 to 16dB, Pin=18dBm)

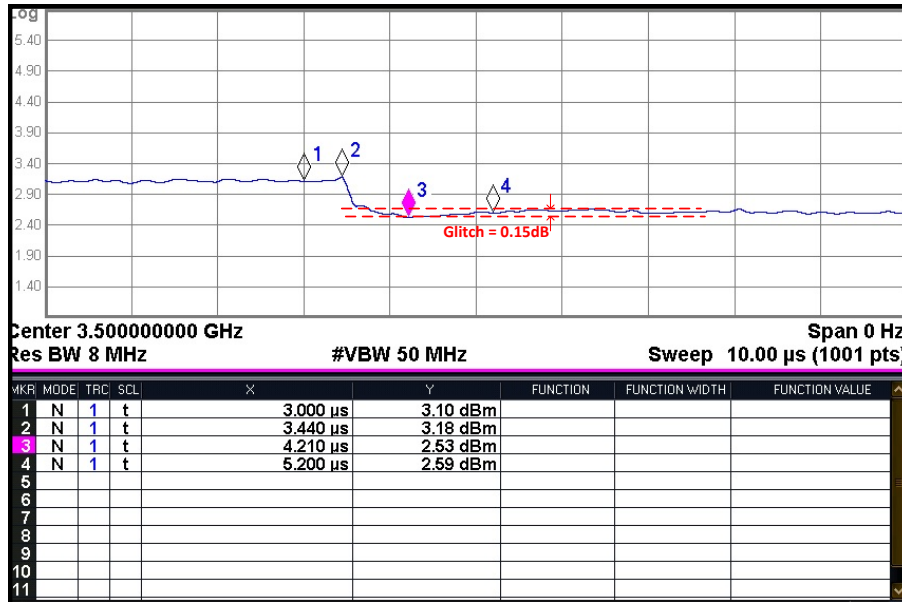
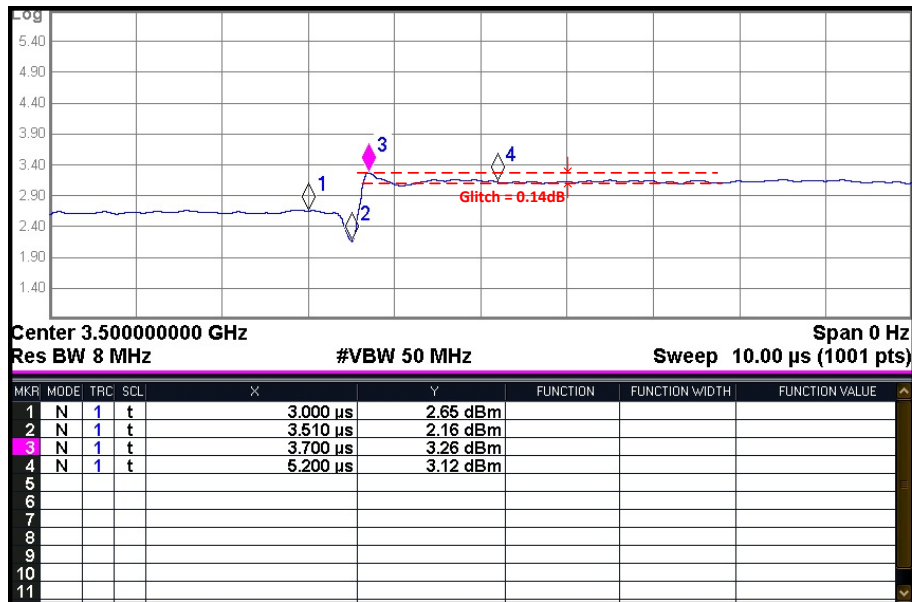
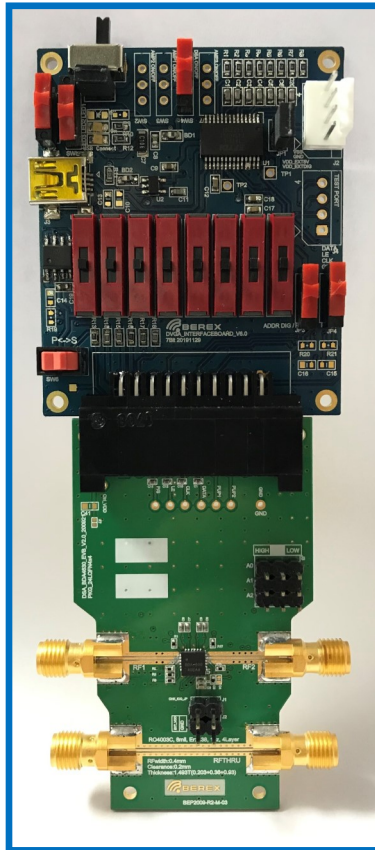


Figure 33. Attenuation Transient (16 to 15.5dB, Pin=18dBm)



### BDA4630 Evaluation board Kit Description



**Figure 34. BDA4630 EVK**

#### Evaluation board Kit Introduction

BDA4630 Evaluation Kit is made up of a combination of an RF board and an interface board

The schematic of the BDA4630 evaluation RF board is shown in Figure 34. The BDA4630 evaluation RF board is constructed of a 4-layer material with a copper thickness of 0.7 mil on each layer. Every copper layer is separated with a dielectric material. The top dielectric material is 8 mils RO4003. The middle and bottom dielectric materials are FR-4, used for mechanical strength and overall board thickness of approximately 1.63mm.

BDA4630 Evaluation INTERFACE board is assembled with a SP3T switches(D0~D5,LE), SP2T mechanical switch (P/S), and several header & switch.

#### Evaluation Board Programming Using USB Interface

In order to evaluate the BDA4630 performance, the Application Software has to be installed on your computer. And The DSA application software GUI supports Latched Parallel and Serial modes. software can be downloaded from BeRex's website

#### Serial Control Mode

- Set the Address Jumper (A0, A1, A2) to HIGH or LOW (Refer to Address Table 7)
- Connect directly the Evaluation INTERFACE board USB port(J3) to PC
- Set the direction of P<->S Switch to S direction (P/S Logic HIGH)
- Set the D0~D5, LE switch to the middle position.
- Operate the 0~31.5dB attenuation state in GUI and then control the DSA

#### Latched Parallel Control Mode

- Connect directly the Evaluation INTERFACE board USB port(J3) to PC
- Set the direction of P<->S Switch to P direction (P/S Logic LOW)
- Set the D0~D5, LE switch to the middle position.
- Operate the 0~31.5dB attenuation state in GUI and then control the DSA

#### Direct Parallel Control Mode

- Set the direction of P<->S Switch to P direction (P/S Logic LOW)
- Set LE switch to the LOW Position
- For the setting to attenuation state, D0~D5 switches can be combined in manually program, refer to Table 9.

Please refer to user manual for more detailed operation method of BDA4630 EVK.

### BDA4630 Evaluation board Kit Description

Figure 35. Evaluation Board Kit Schematic Diagram

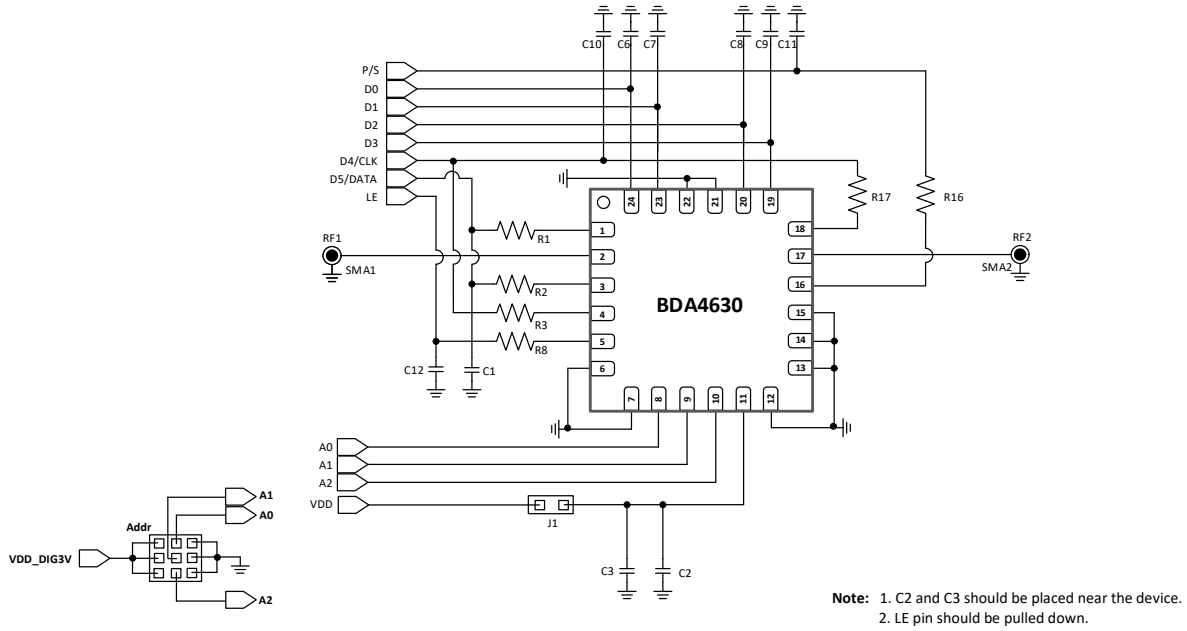


Figure 36. Evaluation Board PCB Layout Information 50Ω

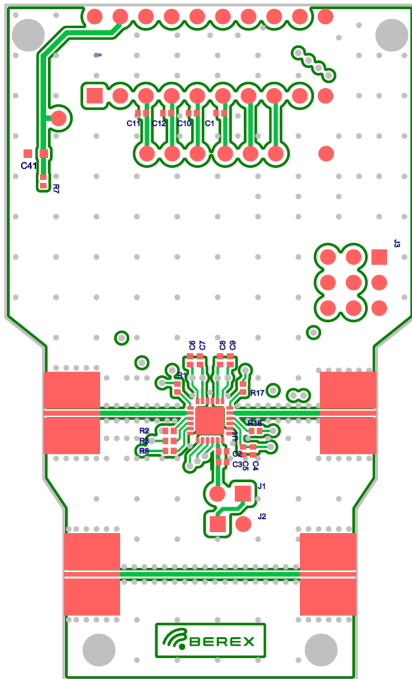


Table 11. Bill of Material - Evaluation Board

No.	Ref Des	Part Qty	Value	Description	Remark
1	C1,C2,C6-C12	9	100pF	CAP, 0402, CHIP Ceramic, ±0.25%	
2	C3	1	100nF	CAP, 0402, CHIP Ceramic, ±0.25%	
2	R16,C4	2	0 ohm	RES, 0402, CHIP, ±5%	
3	R1,R2,R3,R8,R17	5	1k ohm	RES, 0402, CHIP, ±5%	
4	C41,R7	2	NC		
5	SMA1, SMA2	2	CON	SMA END LAUNCH	
6	U1	1	Chip	DSA, BDA4630 QFN4x4 24L	

Figure 37. Evaluation Board PCB Layer Information 50Ω

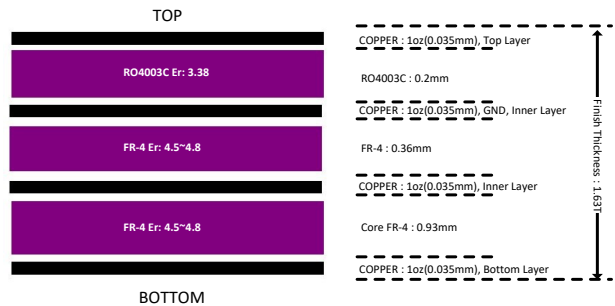
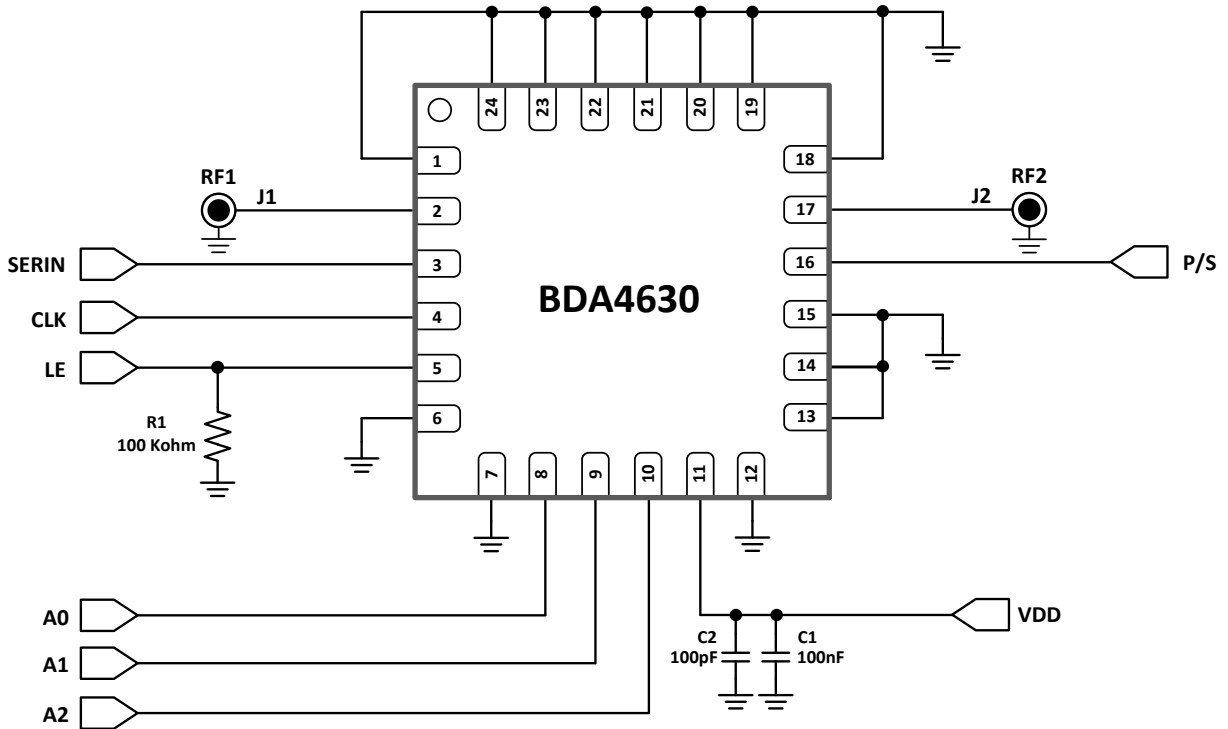
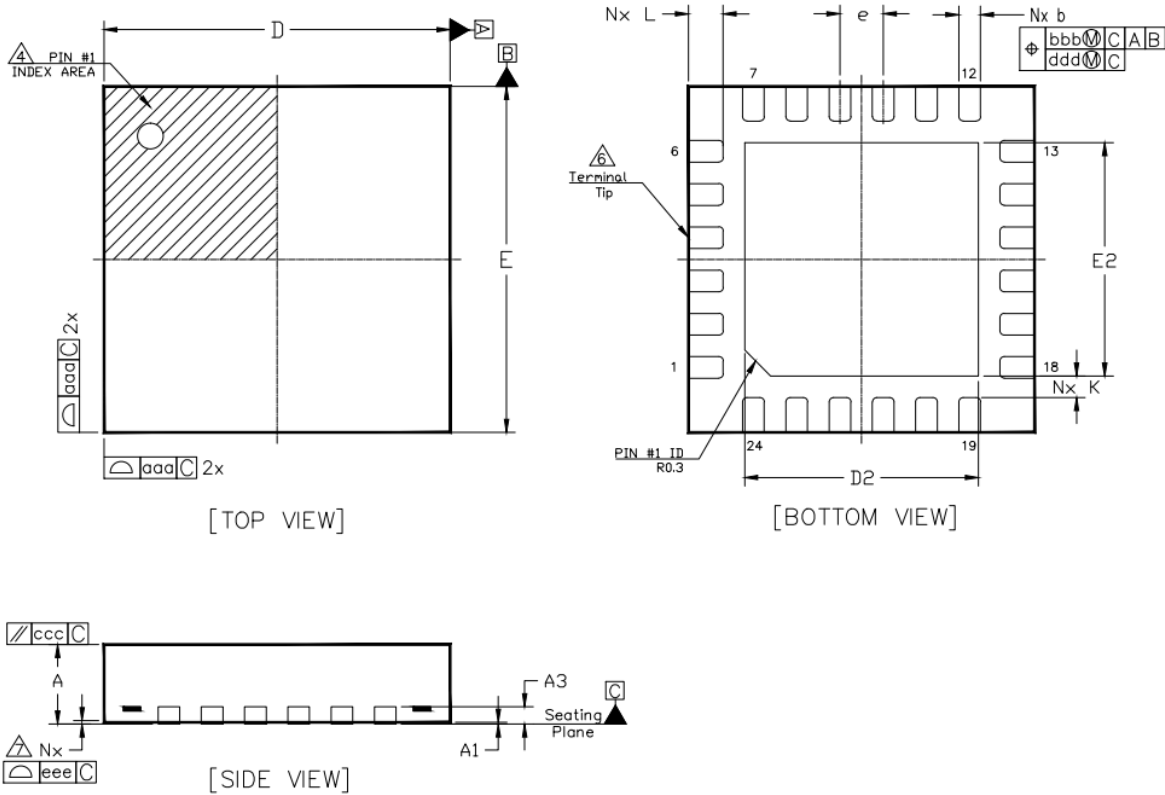


Figure 38. Recommended Serial mode Application Circuit Schematic



- Note:**
1. C1 and C2 should be placed near the device.
  2. Recommended to add pull-down resistor(R1) at the LE pin.
  3. Addressable Pin A0,A1,A2 can be set according to the specified address. If the specified address is 000, All addressable pin(A0,A1,A2) should be grounded.

Figure 39. Packing Outline Dimension



**NOTE :**

1. Dimensioning and tolerancing conform to ASME Y14.5-2009.
2. All dimensions are in millimeters.
3. N is the total number of terminals.
4. The location of the marked terminal #1 identifier is within the hatched area.
5. ND and NE refer to the number of terminals on each D and E side respectively.
6. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has a radius on the other end of it, dimension b should not be measured in that radius area.
7. Coplanarity applies to the terminals and all other bottom surface metallization

Dimension Table				
Symbol	Thickness			NOTE
	MINIMUM	NOMINAL	MAXIMUM	
A	0.80	0.90	1.00	
A1	0.00	0.02	0.05	
A3	---	0.203 Ref	---	
b	0.2	0.25	0.3	6
D		4.0 BSC		
E		4.0 BSC		
e		0.5 BSC		
D2	2.65	2.70	2.75	
E2	2.65	2.70	2.75	
K	0.2	---	---	
L	0.3	0.4	0.5	
aaa		0.05		
bbb		0.10		
ccc		0.10		
ddd		0.05		
eee		0.08		
N		24		3
NE		6		5



Figure 40. Recommend Land Pattern

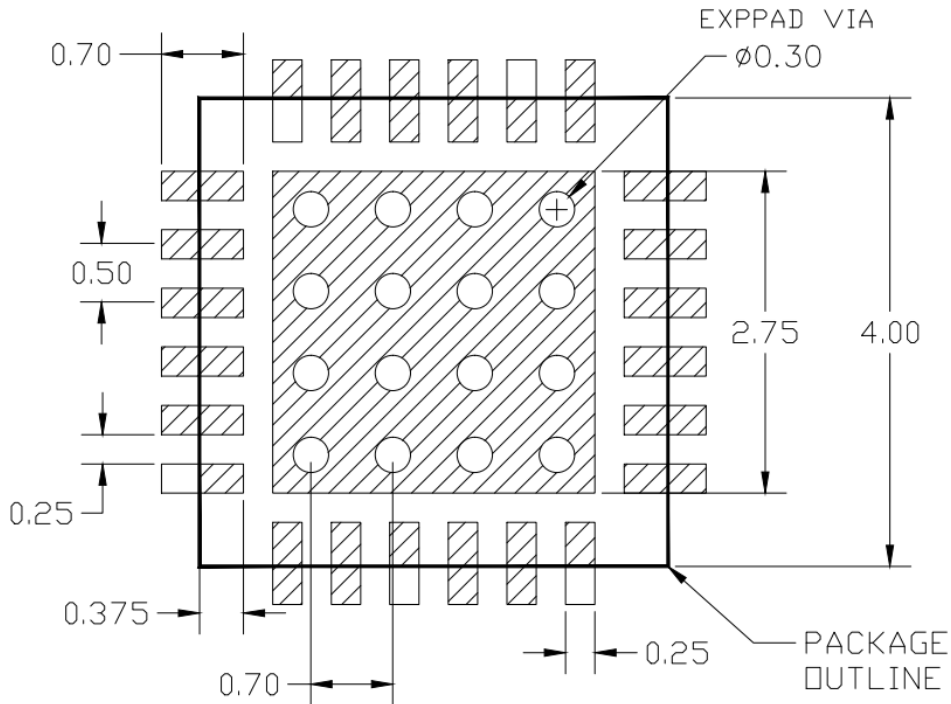
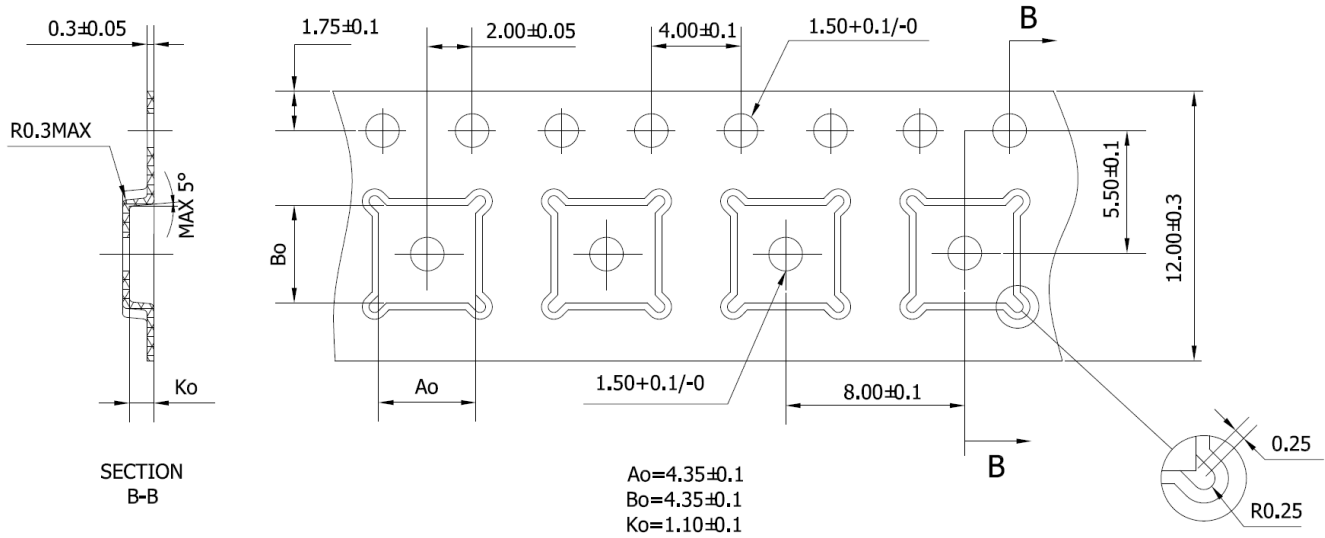


Figure 41. Package Marking



Marking information:	
BDA4630	Device Name
YY	Year
WW	Work Week
XX	LOT Number

Figure 42. Tape & Reel



NOTES:

- 1 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE  $\pm 0.2$
- 2 CAMBER IN COMPLIANCE WITH EIA 481
- 3 POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE

Packaging information:	
Tape Width	12mm
Reel Size	7inch
Device Cavity Pitch	8mm
Devices Per Reel	1k

**Lead plating finish**

100% Tin Matte finish

(All BeRex products undergoes a 1 hour, 150 degree C, Anneal bake to eliminate thin whisker growth concerns.)

**MSL / ESD Rating**

**ESD Rating:** Class 1C  
**Value:** 1000V  
**Test:** Human Body Model (HBM)  
**Standard:** JEDEC Standard JS-001-2017

**ESD Rating:** Class C4  
**Value:** 1000V  
**Test:** Charged Device Model (CDM)  
**Standard:** JEDEC Standard JESD22-C101F

**MSL Rating:** **Level 1 at +260°C convection reflow**  
**Standard:** JEDEC Standard J-STD-020



Proper ESD procedures should be followed when handling this device.

**RoHS Compliance**

This part is compliant with Restrictions on the use of certain Hazardous Substances in Electrical and Electronic Equipment (RoHS) Directive 2011/65/EU as amended by Directive 2015/863/EU.

This product also is compliant with a concentration of the Substances of Very High Concern (SVHC) candidate list which are contained in a quantity of less than 0.1%(w/w) in each components of a product and/or its packaging placed on the European Community market by the BeRex and Suppliers.

**NATO CAGE code:**

<b>2</b>	<b>N</b>	<b>9</b>	<b>6</b>	<b>F</b>
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