TA9210D – 12.5W CW, 30 - 4000MHz GaN Power Transistor

1.0 Features

- Small signal gain @ 800MHz: 18dB
- Large signal gain @ 800MHz: 13.5dB
- PSAT @ 800MHz: 41.5dBm
- PAE @ PSAT @ 800MHz: >55%
- 28V – 32V Typical operation
- Operating frequency: 30MHz to 2.7GHz

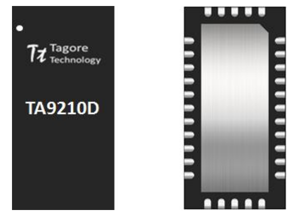

Figure 1.1 Device Image
(32 Pin 3×6×0.8mm QFN Package)

2.0 Applications

- Private mobile radio handsets
- Public safety radios
- Cellular infrastructure
- Military radios

RoHS/REACH/Halogen Free Compliance

3.0 Description

The TA9210D is a broadband capable 12.5W GaN power transistor covering 30MHz to 2.7GHz frequency band with a single match. TA9210D is usable upto 4GHz. The input and output can be matched for best power and efficiency for the desired band.

The TA9210D is packaged in a compact, low cost Quad Flat No lead (QFN) 3x6x0.8mm, 32 leads plastic package.

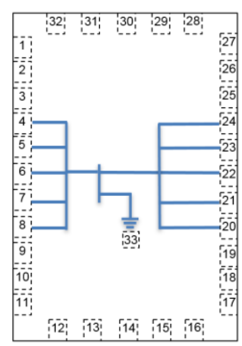

Figure 3.1 Function Block Diagram
(Top View)

4.0 Ordering Information

Table 4.1 Ordering Information

Base Part Number	Package Type	Form	Qty	Reel Diameter	Reel Width	Orderable Part Number
TA9210D	32 Pin 3×6×0.8mm QFN	Tape and Reel	1000	13" (330mm)	18mm	TA9210DMTRPBF
Tuned Evaluation Board, 30 - 2600MHz						TA9210D-EVB-A
Tuned Evaluation Board, 1.8 - 2.7GHz						TA9210D-EVB-B

5.0 Pin Description

Table 5.1 Pin Definition

Pin Number	Pin Name	Description
1, 2, 3, 9, 10, 11, 17, 18, 19, 25, 26, 27	NC	No internal connection. Can be grounded
12, 13, 14, 15, 16, 28, 29, 30, 31, 32	GND	No internal connection. Pins should be grounded and connected to the GND slug for improved thermal relief
4, 5, 6, 7, 8	V_{GG} & RF_{IN}	Gate voltage and RF input
20, 21, 22, 23, 24	V_{DD} & RF_{OUT}	Drain voltage and RF output
33[1]	Paddle/Slug	Ground

Note: [1] The backside ground slug of the device must be grounded directly to the ground plane through multiple vias to ensure proper operation. Adequate heatsinking required.

6.0 Absolute Maximum Ratings

Table 6.1 Absolute Maximum Ratings @T_A=+25°C Unless Otherwise Specified

Parameter	Symbol	Value	Unit
Electrical Ratings			
Breakdown voltage	V_{DS}	+120	V
Gate voltage	V_{GS}	-10 to +2.0	V
Drain current	I_{DS}	1.5	A
Gate current	I_{GS}	4	mA
Power dissipation CW	P_{diss}	22	W
RF input power CW, @800MHz	RF_{IN}	30	dBm
Storage Temperature Range	T_{st}	-55 to +150	°C
Operating Temperature Range	T_{op}	-40 to +85	°C
Maximum Junction Temperature	T_J	+225	°C
Thermal Ratings			
Thermal Resistance (junction-to-case) – Bottom side	$R_{\theta JC}$	6.5	°C/W
Thermal Resistance (junction-to-top)	$R_{\theta JT}$	40	°C/W
Soldering Temperature	T_{SOLD}	260	°C
ESD Ratings			
Human Body Model (HBM)	Level 1B	500 to <1000	V
Charged Device Model (CDM)	Level C2A	500 to <750	V
Moisture Rating			
Moisture Sensitivity Level	MSL	1	-

Attention:
Maximum ratings are absolute ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Exceeding one or a combination of the absolute maximum ratings may cause permanent and irreversible damage to the device and/or to surrounding circuit.

7.0 RF Electrical Specifications

Table 7.1 Electrical Specifications @T_A=+25°C Unless otherwise specified;

Parameter	Condition	Minimum	Typical	Maximum	Unit
Small Signal Gain	800MHz		18		dB
Large Signal Gain	P_{OUT} = 41dBm, 800MHz		13.5		dB
P_{SAT}	800MHz		41.5		dBm
Power Added Efficiency (PAE)	P_{OUT} = 41dBm		54		%
Drain Voltage			32		V
Ruggedness	All phase, P_{OUT} = 41dBm	VSWR = 10:1			

Note: Data taken from 30 - 26000MHz broadband reference design (EVB), V_D=+32V; I_{DQ}=50mA, CW

8.0 Recommended Operating Conditions

Table 8.1 Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Drain Voltage	V_{DD}	+12	+32	+34	V
Gate Voltage	V_{GG}	-2.7	-2.52	-2.3	V
Drain Bias Current	I_{DQ}		50		mA
Drain Current	I_{DS}		700		mA
Power Dissipation CW [1]	P_{diss}			20	W
Operating Temperature Range		-40	+25	+85	°C

Note: [1] @TC = +85°C

9.0 Typical Characteristics

9.1 30 - 2600MHz EVB (Vdd = 28V)

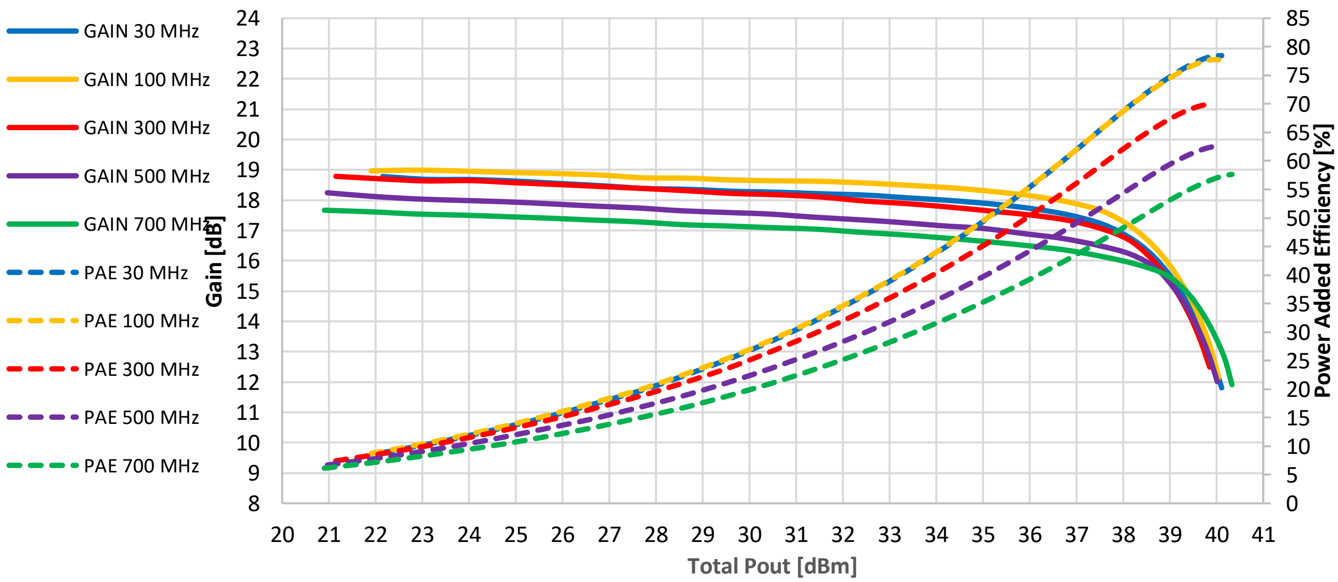

Figure 9.1 Gain and PAE vs P_{OUT} (30-700MHz)
(V_D=28V, I_{DQ}=50mA, CW, T_A=+25°C)

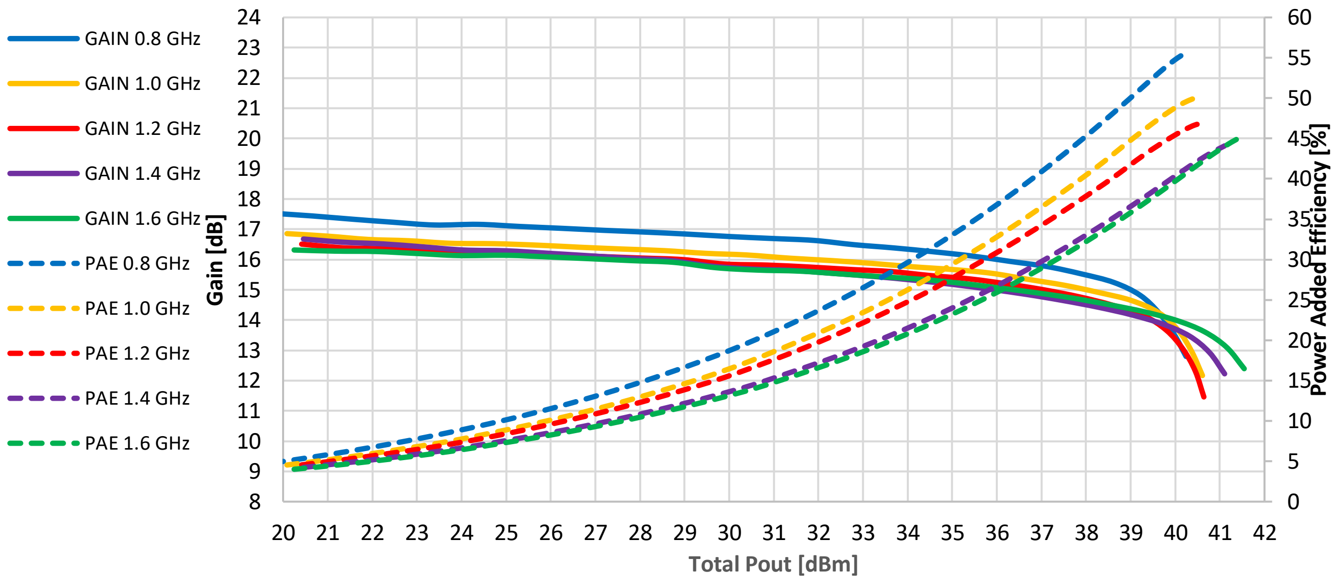

Figure 9.2 Gain and PAE vs P_{OUT} (800-1600MHz)
(V_D=28V, I_{DQ}=50mA, CW, T_A=+25°C)

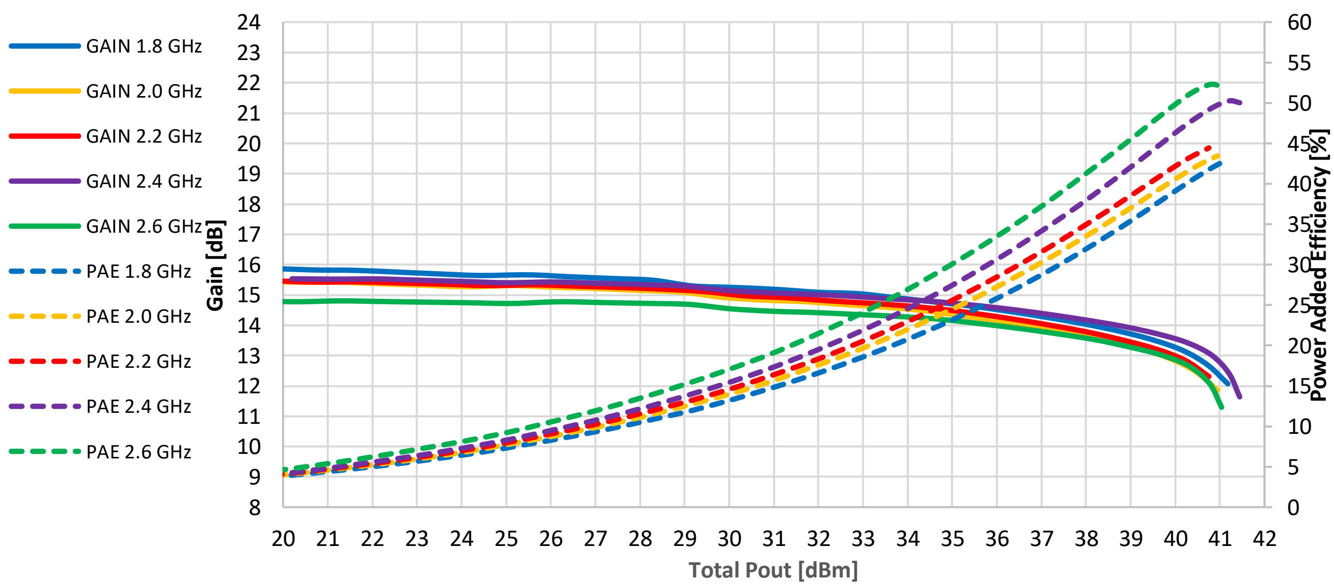

Figure 9.3 Gain and PAE vs P_{OUT} (1800-2600MHz)
(V_D=28V, I_{DQ}=50mA, CW, T_A=+25°C)

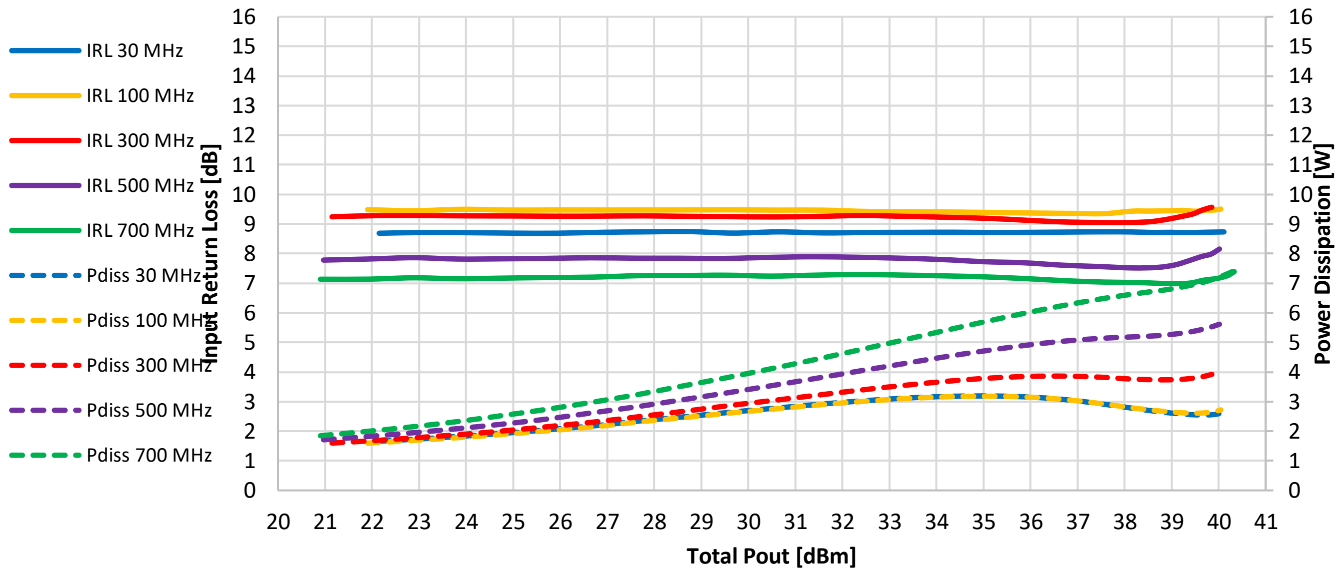

Figure 9.4 IRL and P_{diss} vs P_{OUT} (30-700MHz)
(V_D=28V, I_{DQ}=50mA, CW, T_A=+25°C)

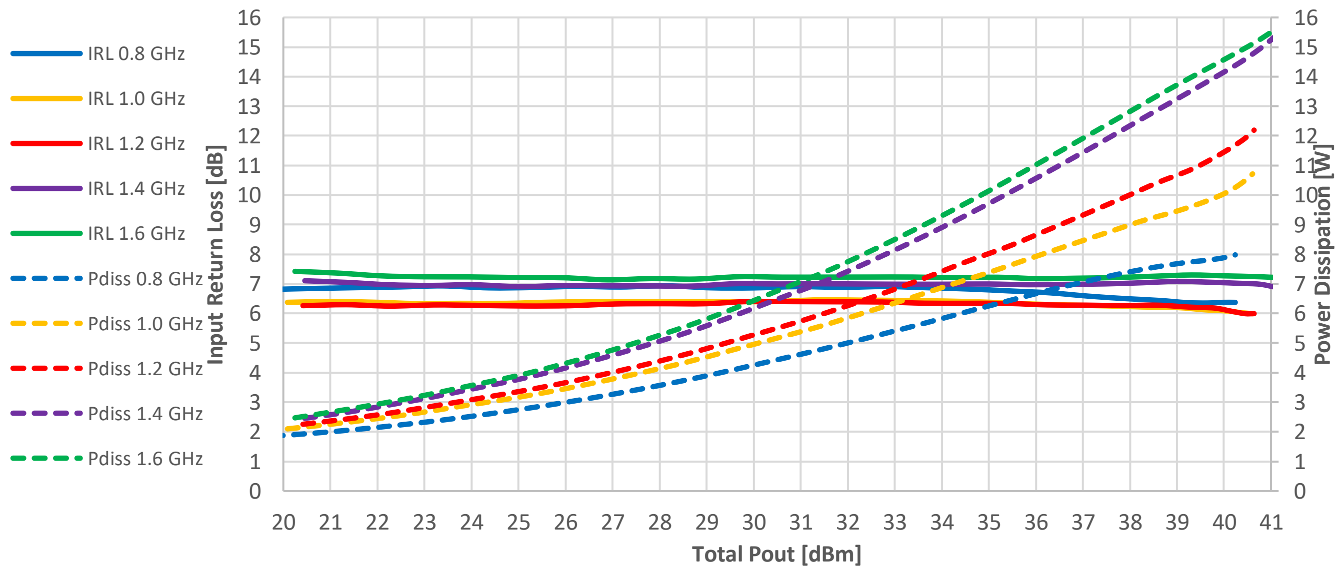

Figure 9.5 IRL and P_{diss} vs P_{OUT} (800-1600MHz)
(V_D=28V, I_{DQ}=50mA, CW, T_A=+25°C)

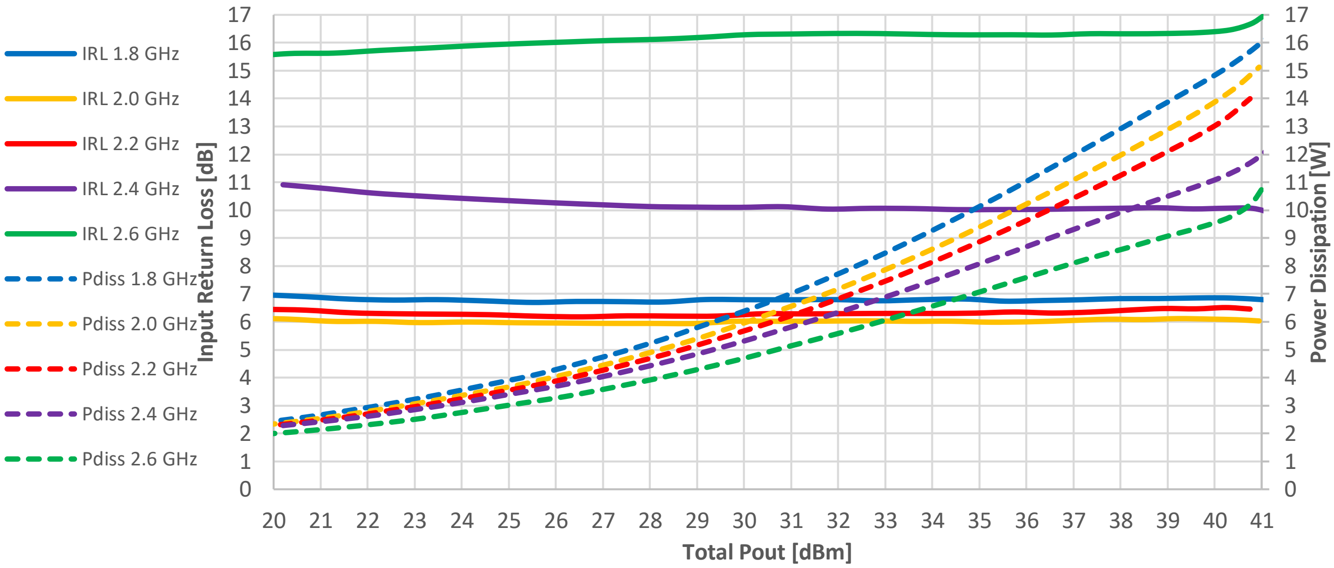

Figure 9.6 IRL and P_{diss} vs P_{OUT} (1800-2600MHz)
(V_D=28V, I_{DQ}=50mA, CW, T_A=+25°C)

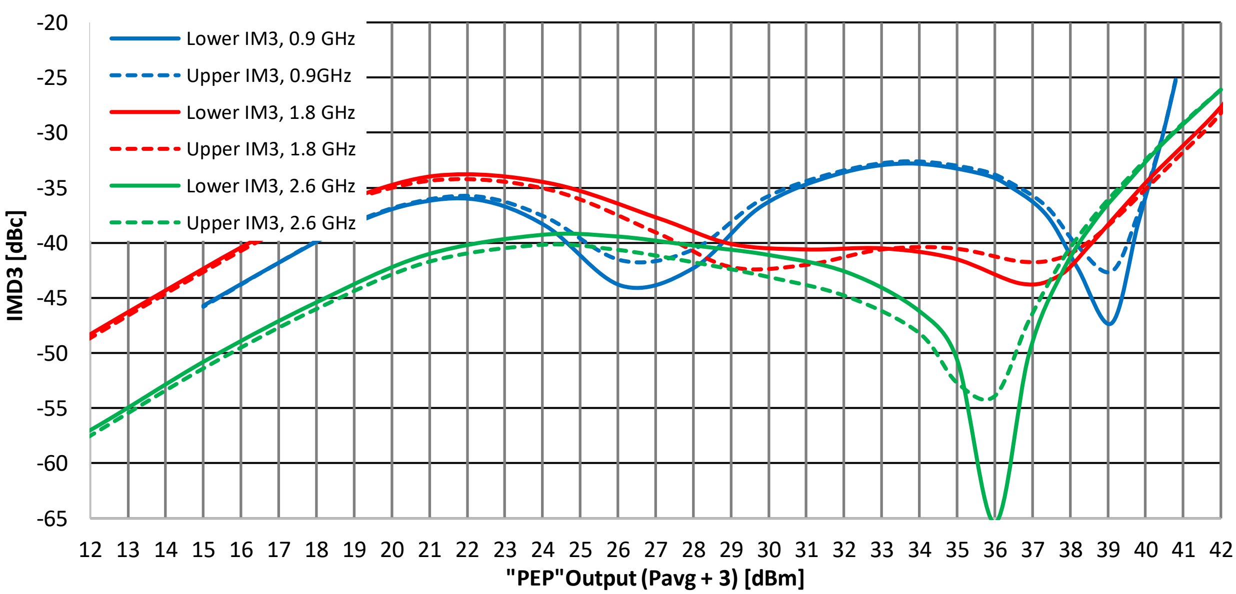

Figure 9.7 IMD3 vs P_{OUT}
(V_D=28V, I_{DQ}=50mA, CW, Fsp=200kHz, T_A=+25°C)

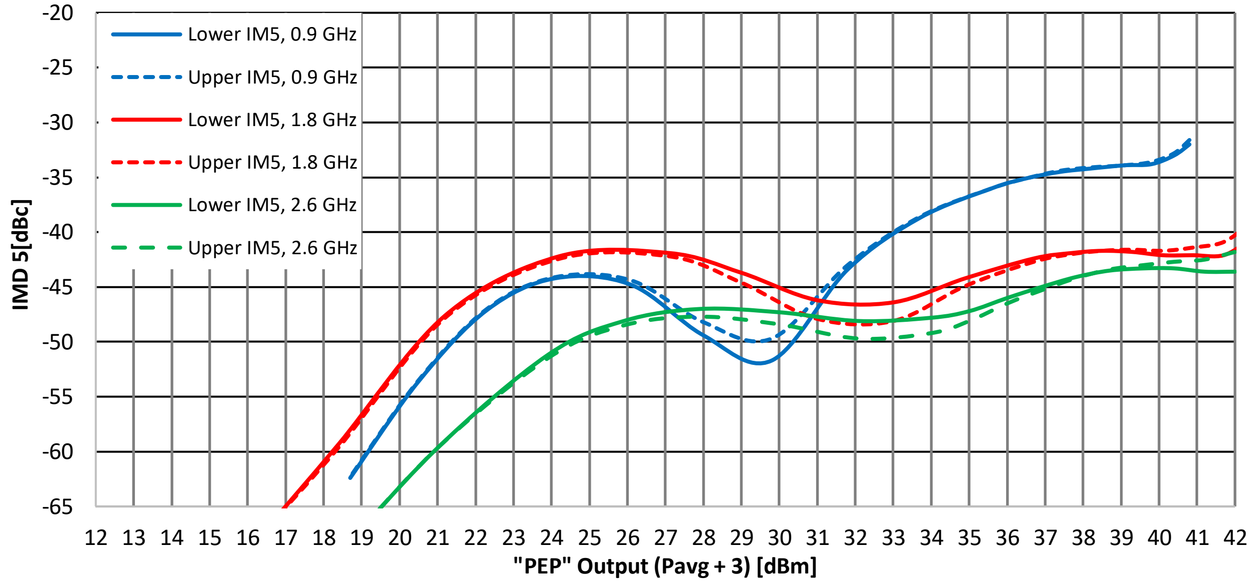

Figure 9.8 IMD5 vs P_{OUT}

(V_D=28V, I_{DQ}=50mA, CW, Fsp=200kHz, T_A=+25°C)

9.2 30 - 2600MHz EVB (Vdd = 32V)

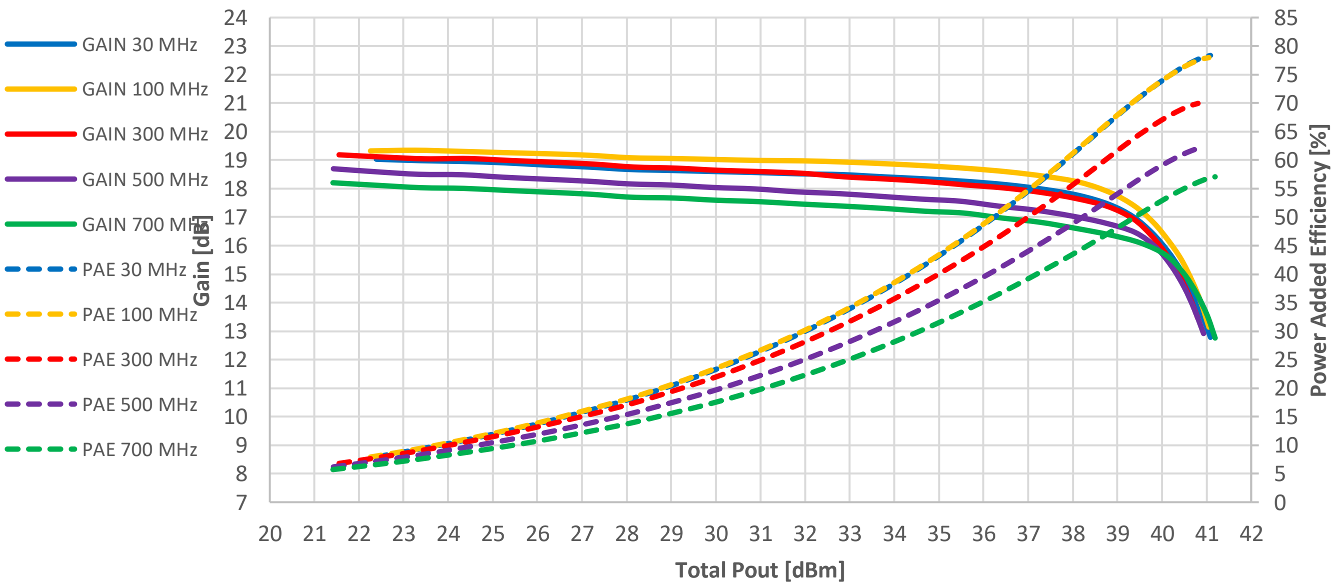

Figure 9.9 Gain and PAE vs P_{OUT} (30-700MHz)

(V_D=32V, I_{DQ}=50mA, CW, T_A=+25°C)

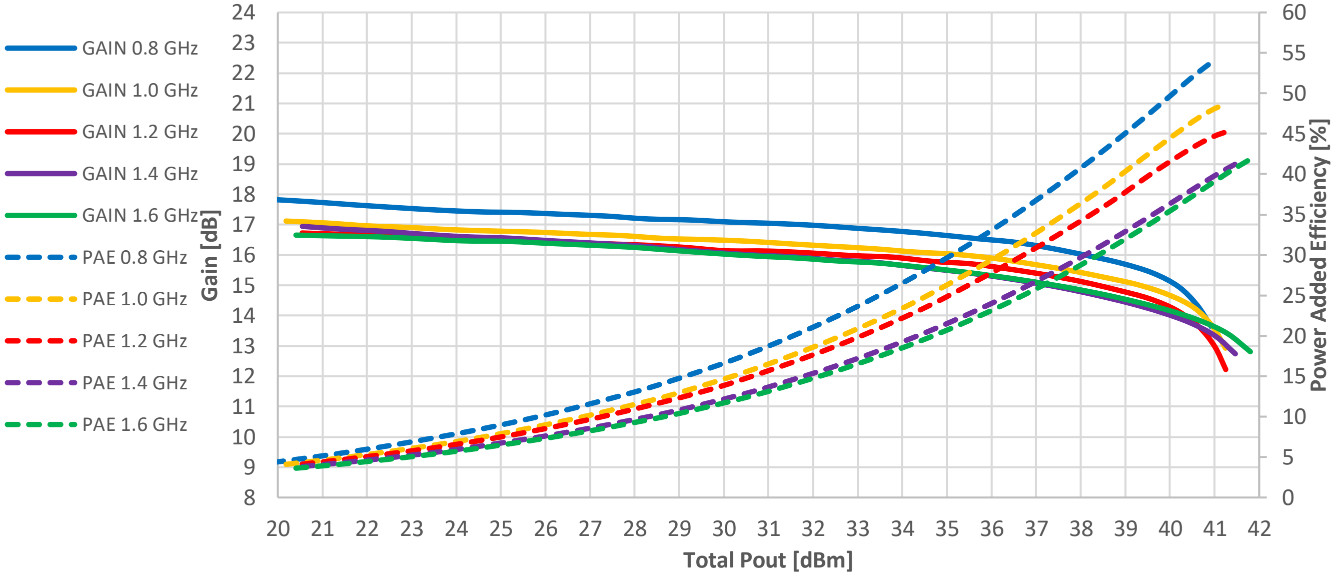

Figure 9.10 Gain and PAE vs P_{OUT} (800-1600MHz)
(V_D=32V, I_{DQ}=50mA, CW, T_A=+25°C)

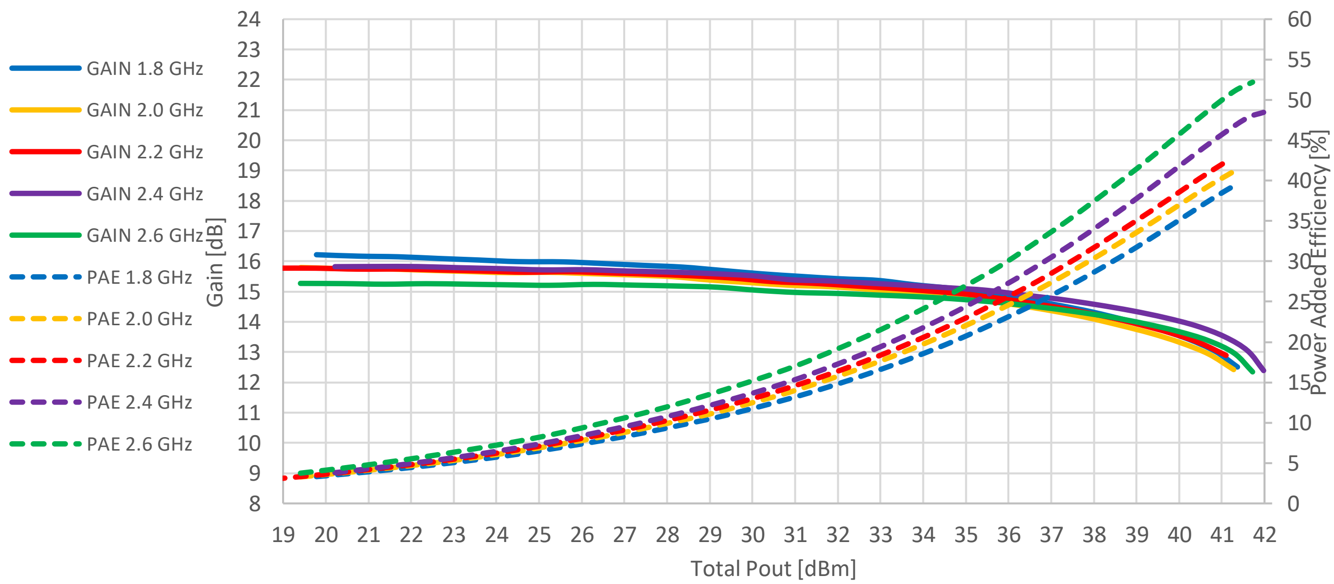

Figure 9.11 Gain and PAE vs P_{OUT} (1800-2600MHz)
(V_D=32V, I_{DQ}=50mA, CW, T_A=+25°C)

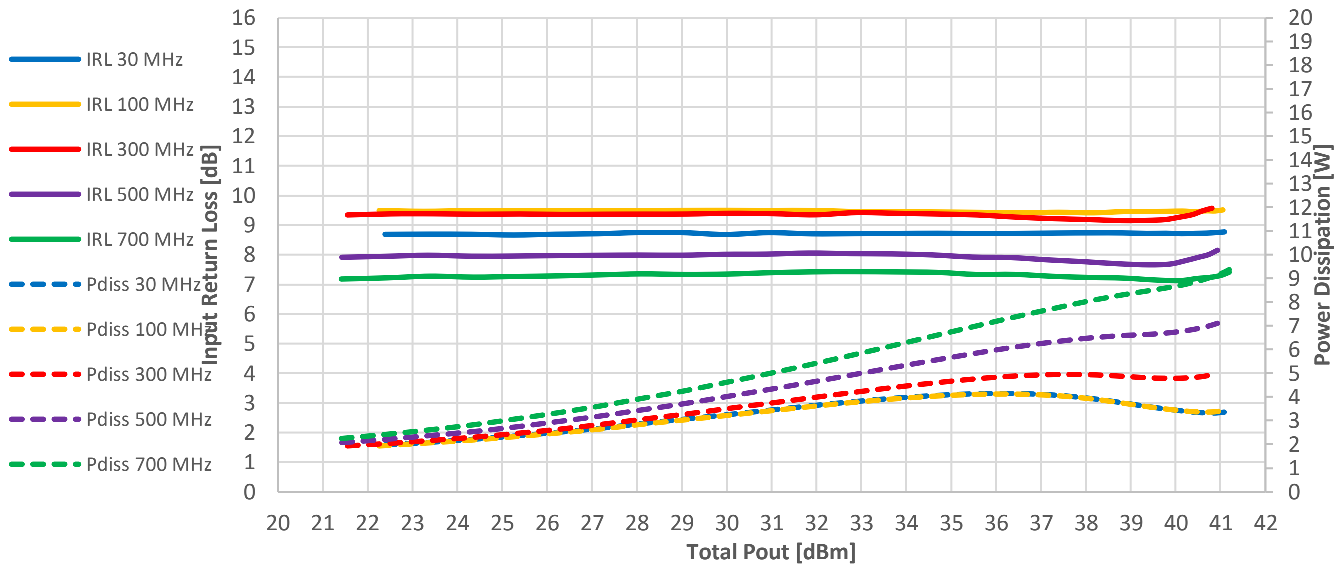

Figure 9.12 IRL and P_{diss} vs P_{OUT} (30-700MHz)
(V_D=32V, I_{DQ}=50mA, CW, T_A=+25°C)

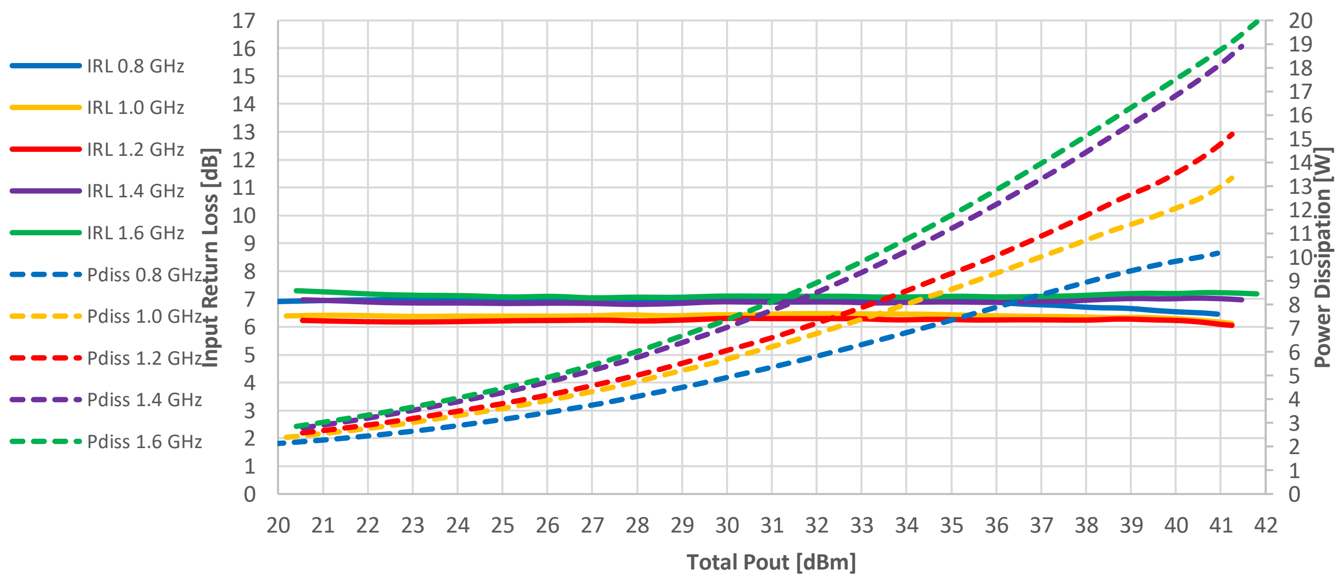

Figure 9.13 IRL and P_{diss} vs P_{OUT} (800-1600MHz)
(V_D=32V, I_{DQ}=50mA, CW, T_A=+25°C)

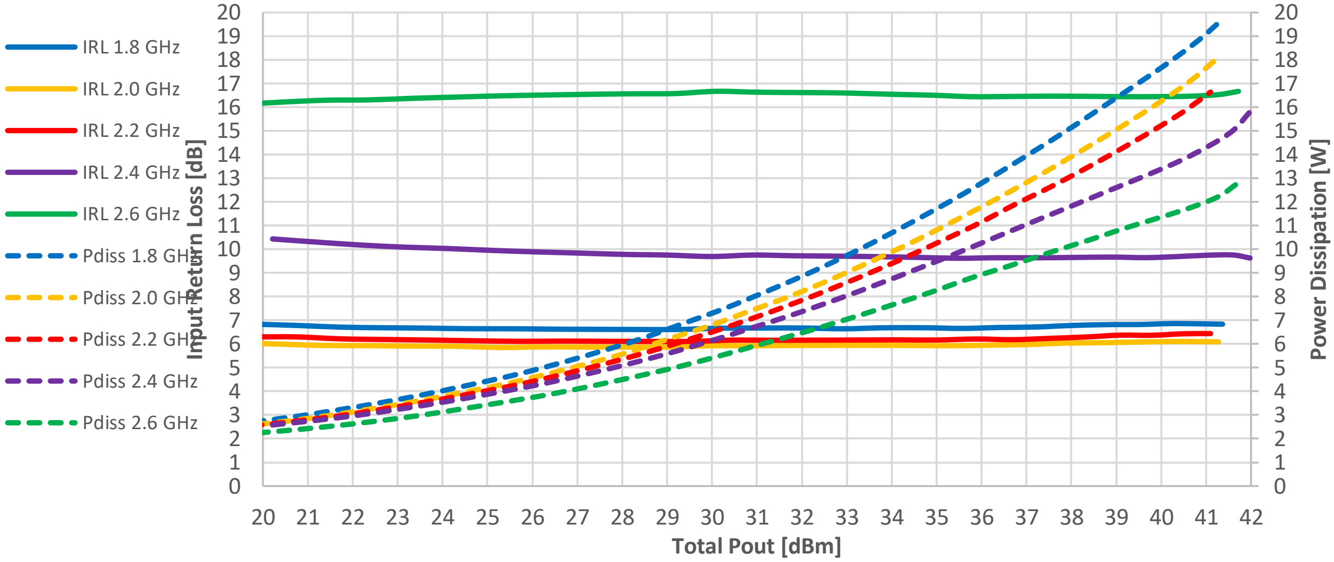

Figure 9.14 IRL and P_{diss} vs P_{OUT} (1800-2600MHz)
(V_D=32V, I_{DQ}=50mA, CW, T_A=+25°C)

10.0 1.8 – 2.7GHz EVB (Vdd = 32V)

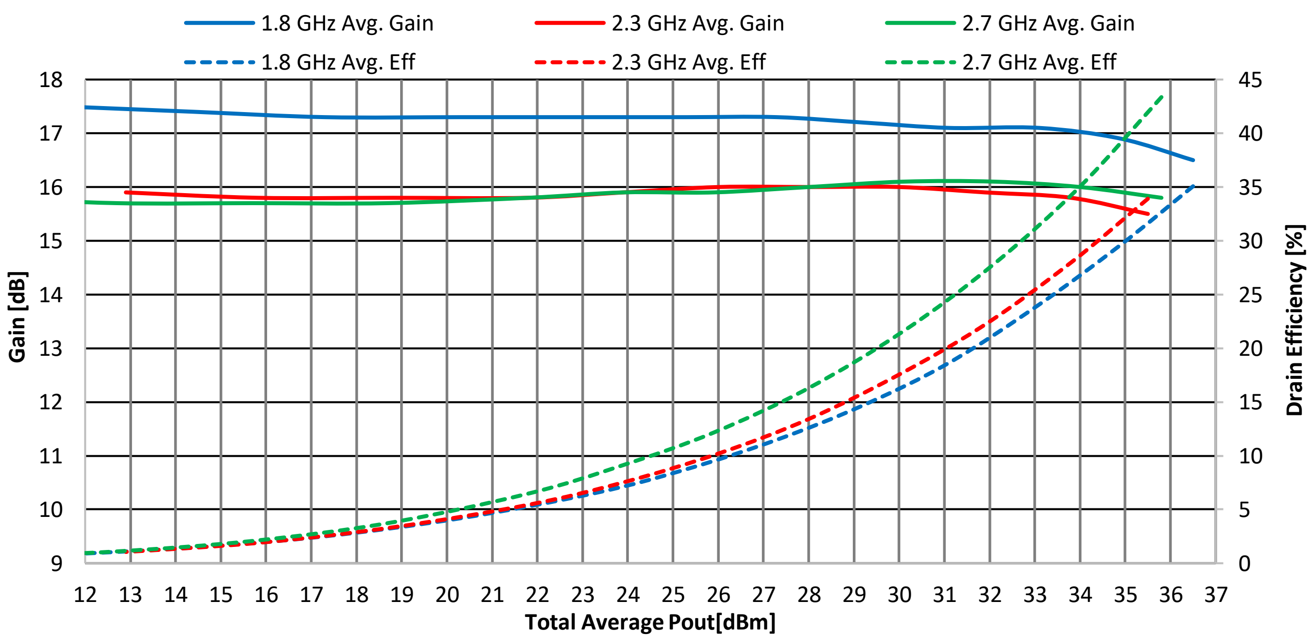

Figure 10.1 Gain and Efficiency vs P_{OUT}
(V_D=32V, I_{DQ}=50mA, LTE, PAPR = 9.5dB, 10MHz BW, T_A=+25°C)

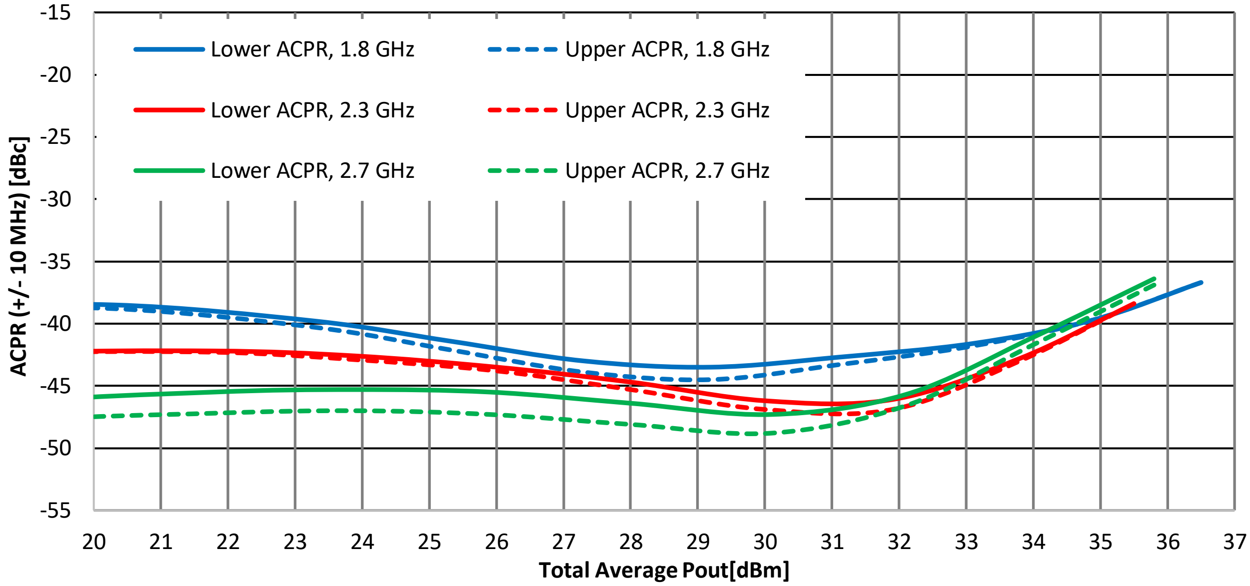

Figure 10.2 ACPR vs P_{OUT}
(V_D=32V, I_{DQ}=50mA, LTE, PAPR = 9.5dB, 10MHz BW, T_A=+25°C)

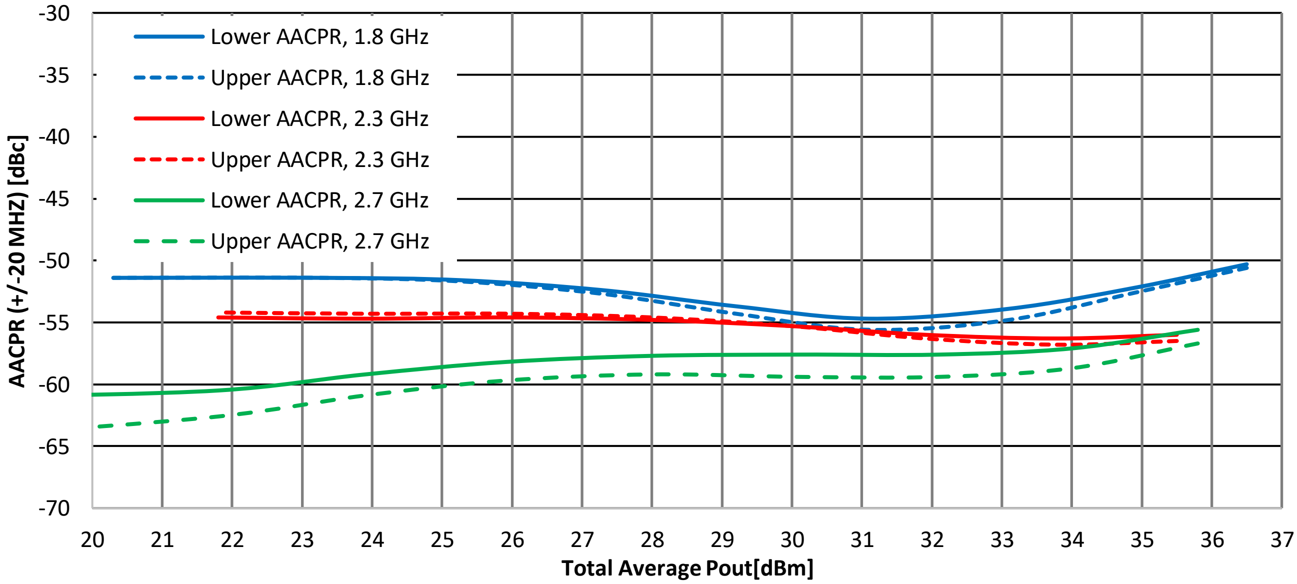

Figure 10.3 AACPR vs P_{OUT}
(V_D=32V, I_{DQ}=50mA, LTE, PAPR = 9.5dB, 10MHz BW, T_A=+25°C)

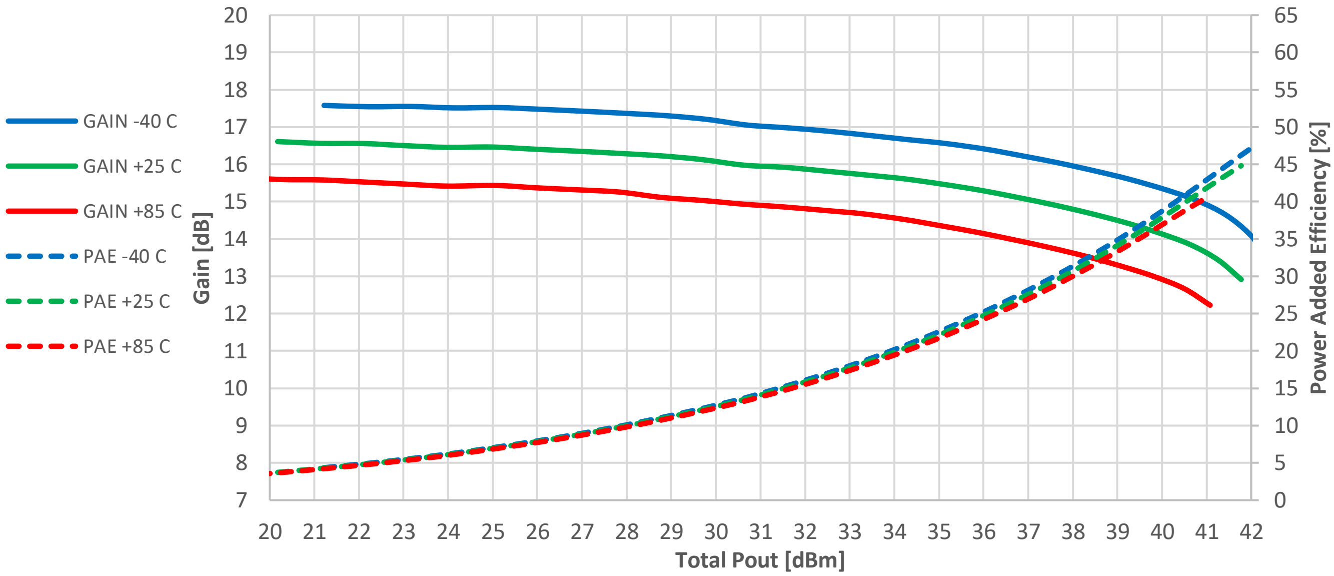

Figure 10.4 Gain and PAE vs P_{OUT} at 1.8GHz over temp
(V_D=32V, I_{DQ}=50mA, CW)

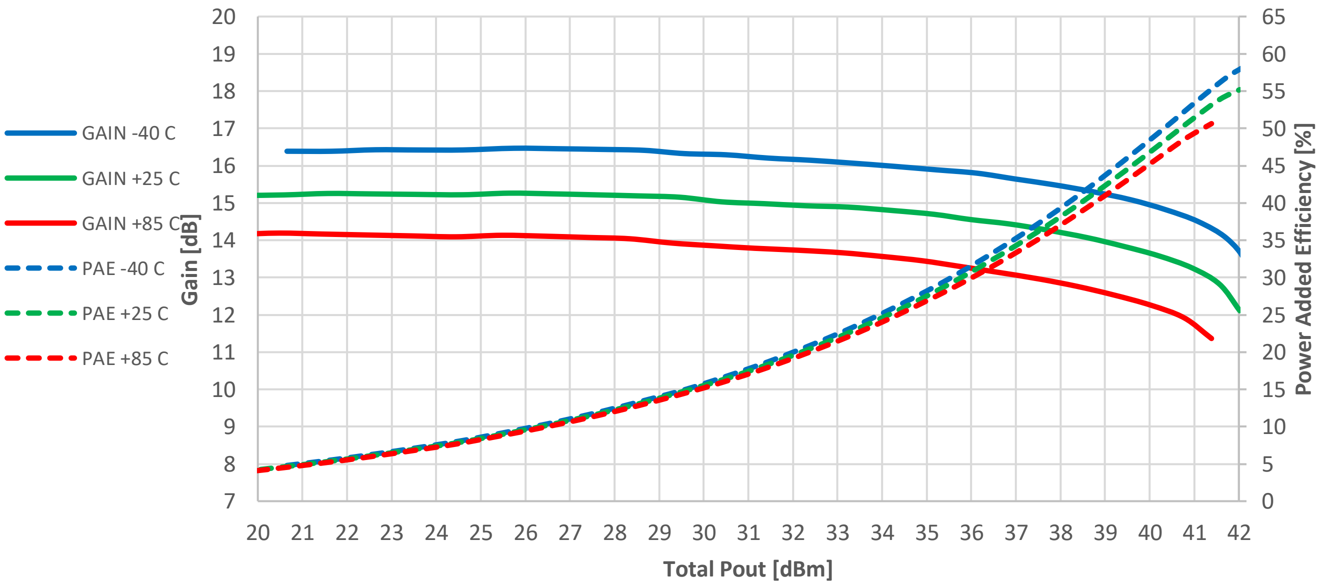

Figure 10.5 Gain and PAE vs P_{OUT} at 2.7GHz over temp
(V_D=32V, I_{DQ}=50mA, CW)

11.0 Bias and Sequencing

Table 11.1 Bias and Sequencing

Turn ON Device	Turn OFF Device
1. Set V_G to -5V 2. Set V_D to +28V 3. Adjust V_G to reach required I_{DQ} current 4. Apply RF power	1. Turn RF power off 2. Turn off V_D 3. Turn off V_G

12.0 Evaluation Boards

12.1 30 - 2600MHz EVB

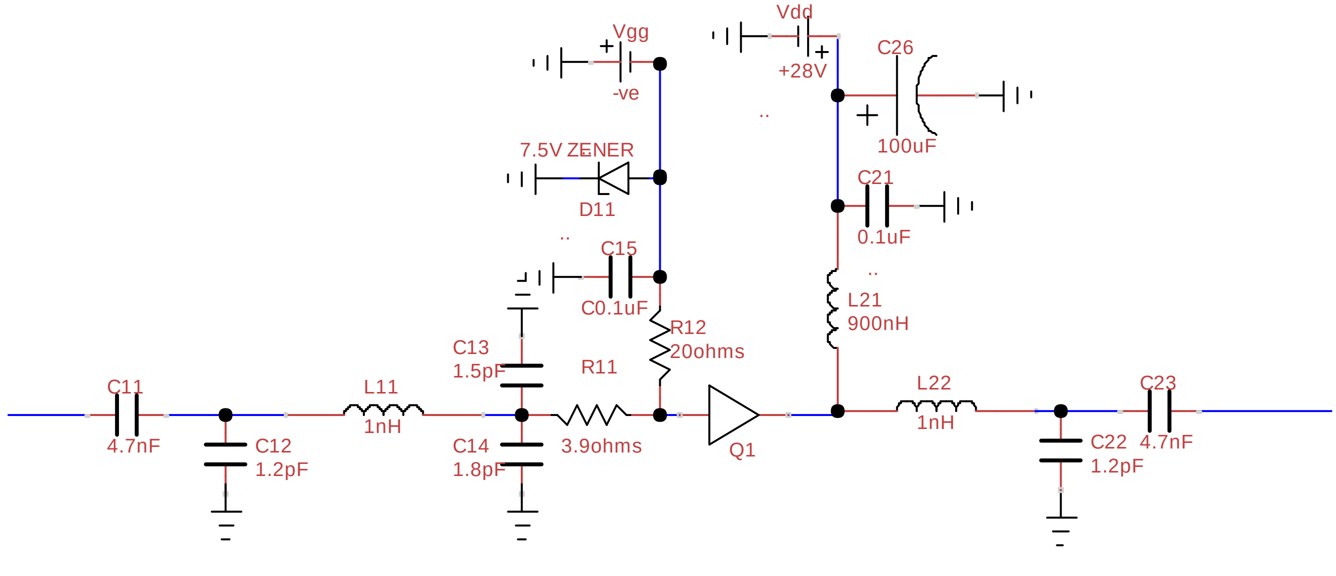

Figure 12.1 Schematic of the 30 - 2600MHz EVB

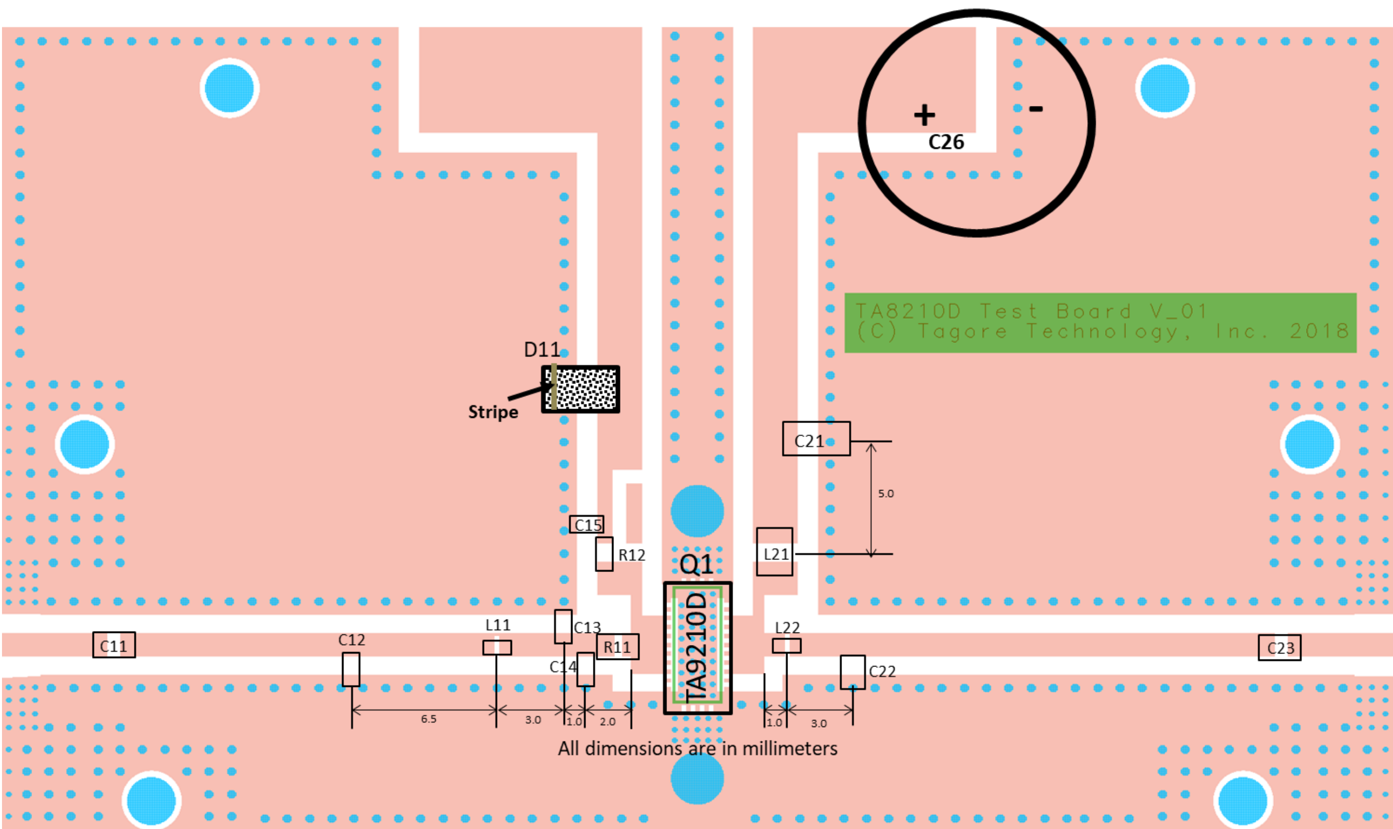

Figure 12.2 Board Layout of the 30 - 2600MHz EVB

Table 12.1 BOM of the 30 - 2600MHz EVB

Component ID	Value	Manufacturer	Recommended Part Number
C11, C23	4.7nF, 50V	Murata	GRM1885C1H472JA01
C12	1.2pF	ATC	600S1R2CT250XT
L11, L22	1.0nH	Coilcraft	0402HP-1N0XGL
L21	900nH	Coilcraft	1008AF-901XJLC
C13	1.5pF	ATC	600S1R5CT250XT
C14	1.8pF	ATC	600S1R8CT250XT
C15	0.1uF, 10V	AVX	0603ZC104K4T2A
C21	0.1uF, 50V	Murata	GRM31C5C1H104JA01L
C22	1.2pF	ATC	800A1R2BT250XT
C26	100uF	Nichicon	UPW1J101MPD1TD
R11	3.9Ω, 250mW	Panasonic	ERJ-PA3J3R9V
R12	20Ω, 250mW	Panasonic	ERJ-PA3F20R0V
D11	7.5 V, 0.5W Zener	On Semiconductor	SZMMSZ5236BT 1G
Q1		Tagore Technology	TA9210D
PCB	Rogers RO4350B, 20 mils, 2 oz copper		

12.2 1.8 - 2.7GHz EVB

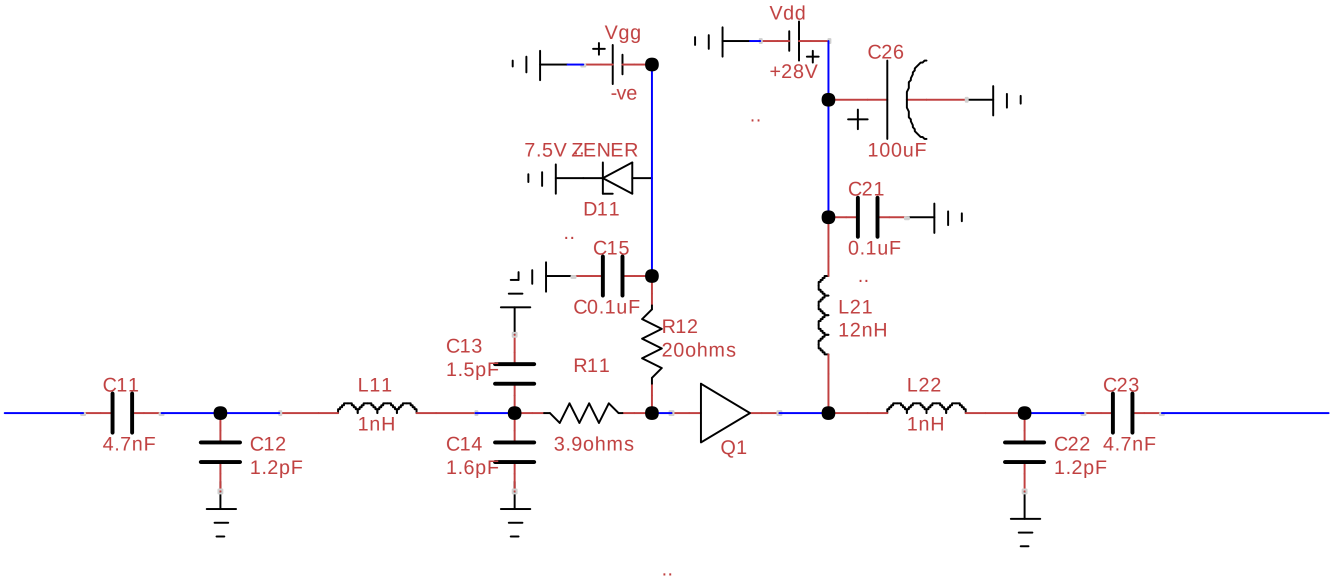

Figure 12.3 Schematic of the 1.8 - 2.7GHz EVB

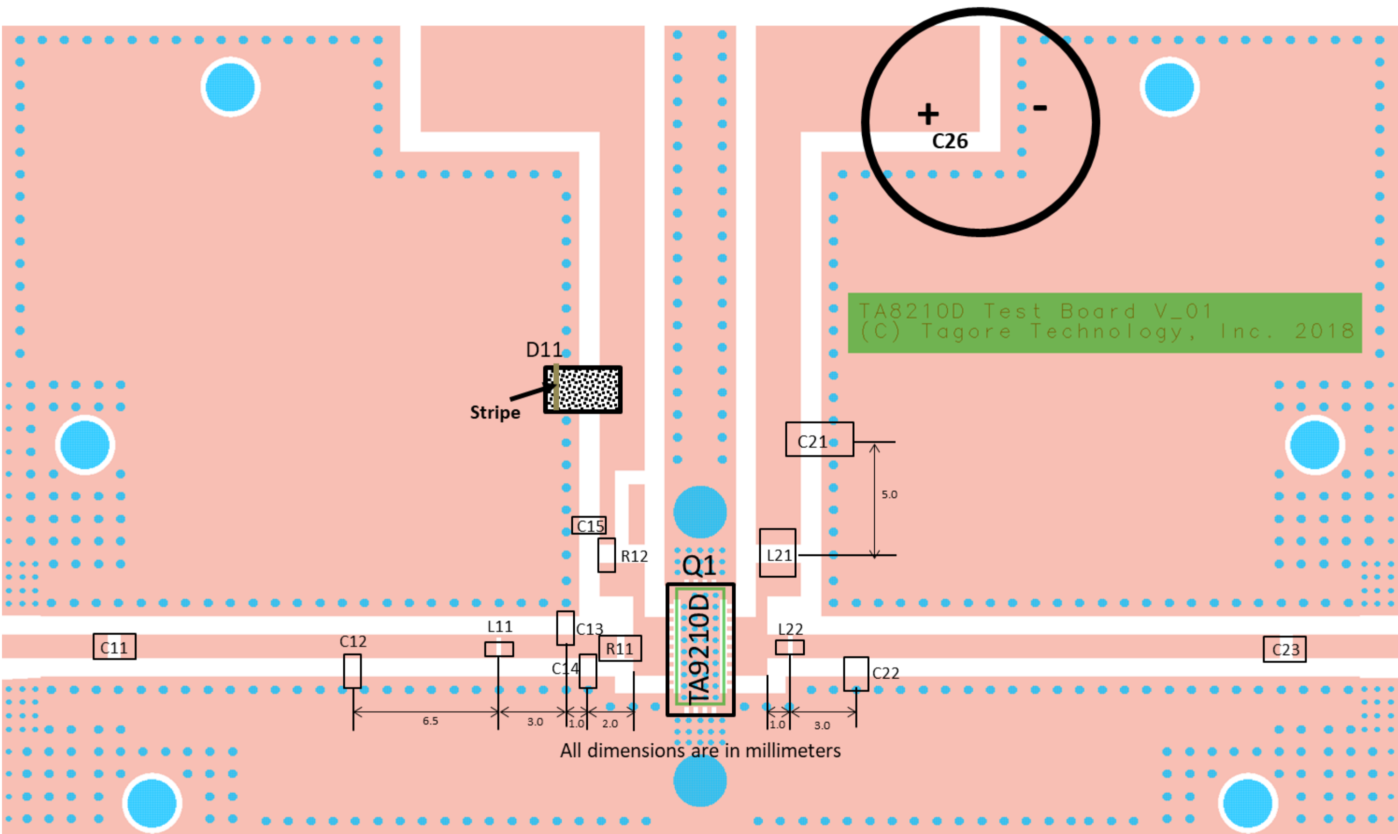

Figure 12.4 Board Layout of the 1.8 - 2.7GHz EVB

Table 12.2 BOM of the 1.8 – 2.7GHz EVB

Component ID	Value	Manufacturer	Recommended Part Number
C11, C23	4.7nF, 50V	Murata	GRM1885C1H472JA01
C12	1.2pF	ATC	600S1R2CT250XT
L11, L22	1.0nH	Coilcraft	0402HP-1N0XJL
L21	12nH	Coilcraft	0603HC-12NXGE
C13	1.5pF	ATC	600S1R5CT250XT
C14	1.6pF	ATC	600S1R6CT250XT
C15	0.1uF, 10V	AVX	0603ZC104K4T2A
C21	0.1uF, 50V	Murata	GRM31C5C1H104JA01L
C22	1.2pF	ATC	800A1R2BT250XT
C26	100uF	Nichicon	UPW1J101MPD1TD
R11	3.9Ω, 250mW	Panasonic	ERJ-PA3J3R9V
R12	20Ω, 250mW	Panasonic	ERJ-PA3F20R0V
D11	7.5 V, 0.5W Zener	On Semiconductor	SZMMSZ5236BT 1G
Q1		Tagore Technology	TA9210D
PCB	Rogers RO4350B, 20 mils, 2 oz copper		

13.0 Device Package Information

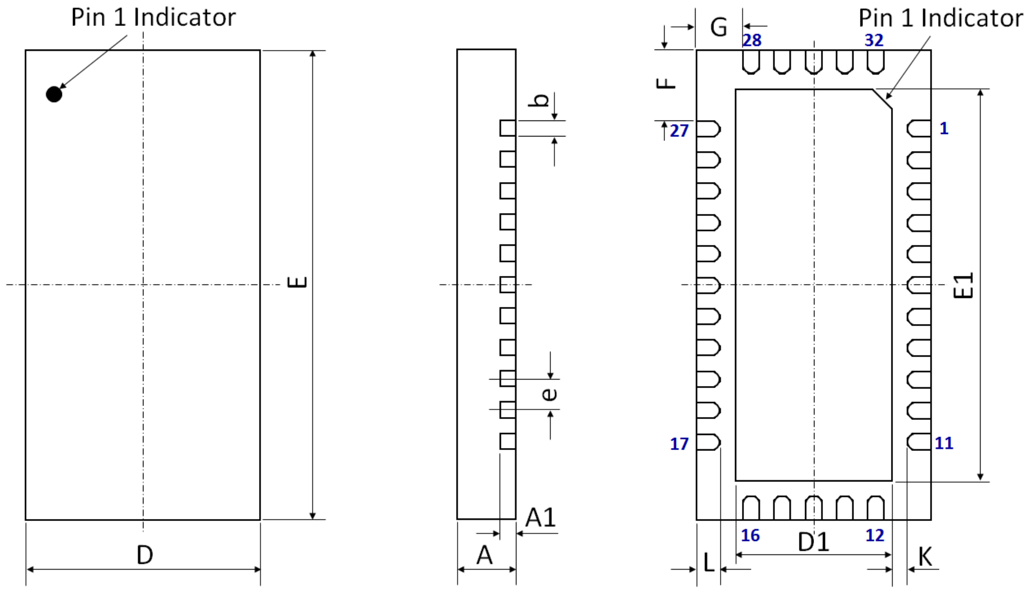

Figure 13.1 Device Package Drawing
(All dimensions are in mm)

Table 13.1 Device Package Dimensions

Dimension (mm)	**Value** (mm)	**Tolerance** (mm)	**Dimension** (mm)	**Value** (mm)	**Tolerance** (mm)
A	0.80	±0.05	E	6.00 BSC	±0.05
A1	0.203	±0.02	E1	5.00	±0.05
b	0.20	+0.05/-0.07	F	0.90	±0.05
D	3.00 BSC	±0.05	G	0.60	±0.05
D1	2.00	±0.05	L	0.25	±0.05
e	0.40 BSC	±0.05	K	0.25	±0.05

Note: Lead finish: Pure Sn without underlayer; Thickness: 7.5µm ~ 20µm (Typical 10µm ~ 12µm)

Attention:
Please refer to application notes *TN-001* and *TN-002* at http://www.tagoretech.com for PCB and soldering related guidelines.

14.0 PCB Land Design

Guidelines:
[1] 2-layer PCB is recommended.
[2] Via diameter is recommended to be 0.2mm to prevent solder wicking inside the vias.
[3] Thermal vias shall only be placed on the center pad.
[4] The maximum via number for the center pad is 4(X)×12(Y)=48.

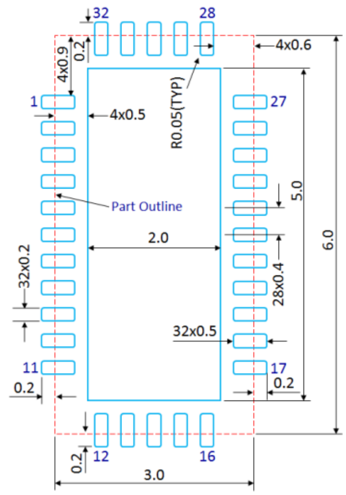

Figure 14.1 PCB Land Pattern
(Dimensions are in mm)

Non-Solder Mask Defined
(Preferred)

Solder Mask Defined

Figure 14.2 Solder Mask Pattern
(Dimensions are in mm)

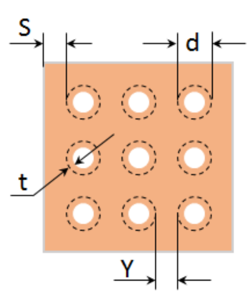

Figure 14.3 Thermal Via Pattern
(Recommended Values: S≥0.15mm; Y≥0.20mm; d=0.2mm; Plating Thickness t=25µm or 50µm)

15.0 PCB Stencil Design

Guidelines:

[1] Laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.

[2] Stencil thickness is recommended to be 125µm.

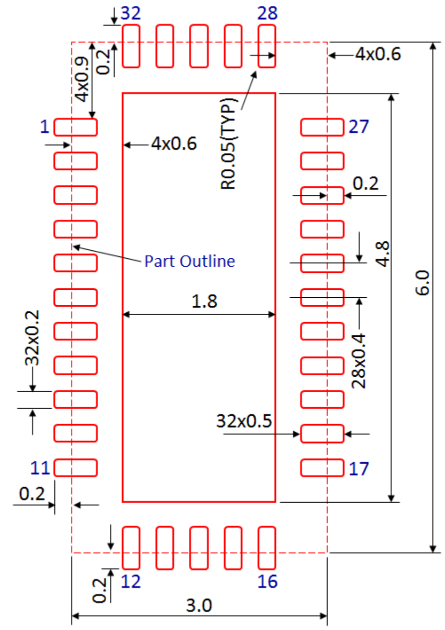

Figure 15.1 Stencil Openings
(Dimensions are in mm)

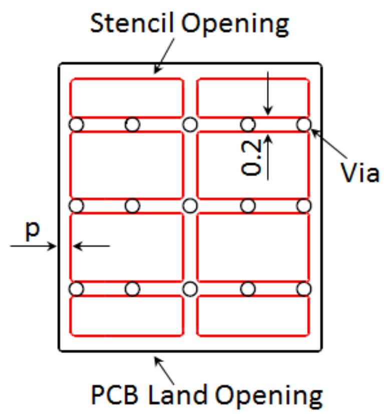

Figure 15.2 Stencil Openings Shall not Cover Via Areas If Possible
(Dimensions are in mm)

16.0 Tape and Reel Information

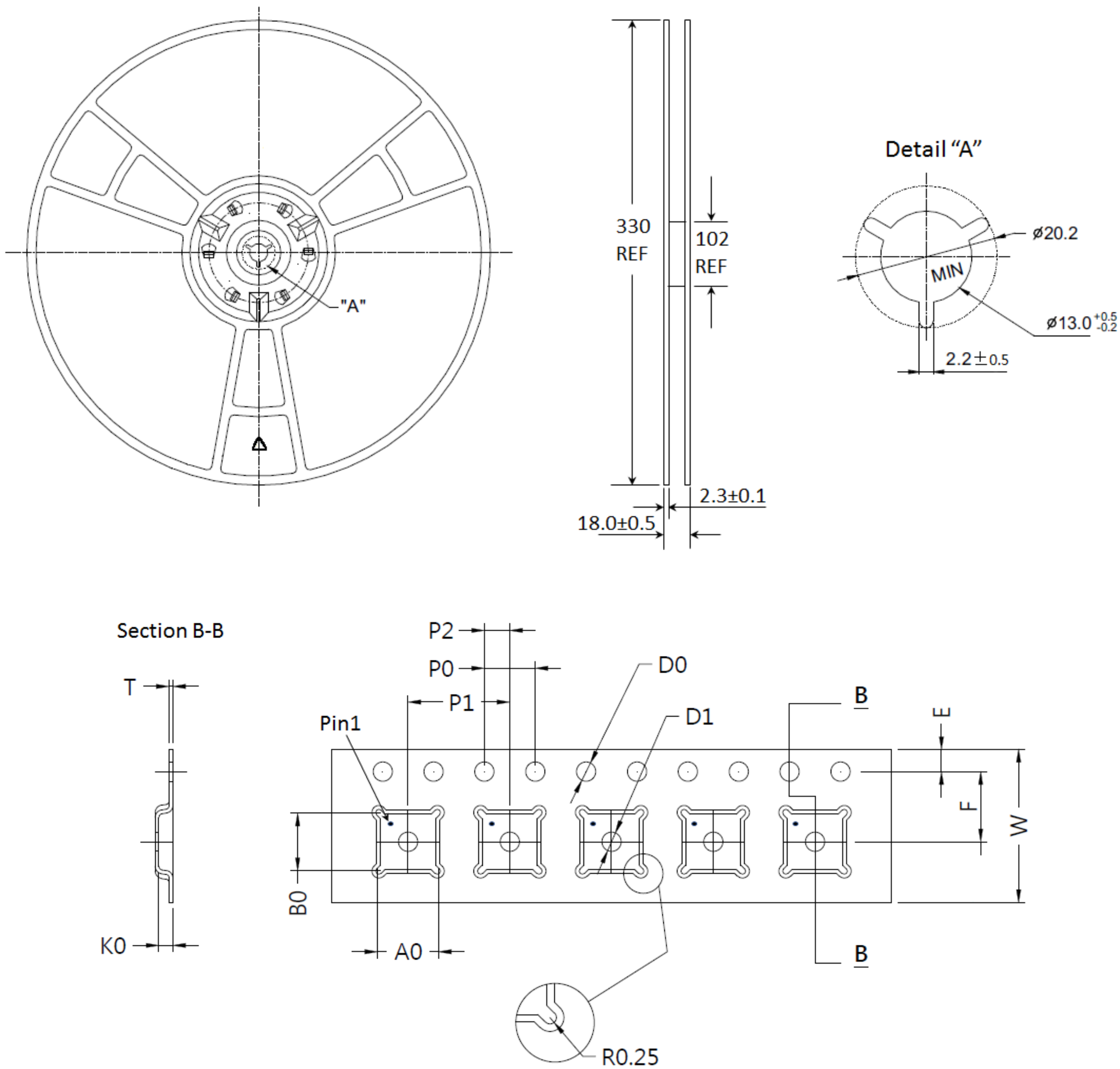

Figure 16.1 Tape and Reel Drawing

Table 16.1 Tape and Reel Dimensions

Dimension (mm)	**Value** (mm)	**Tolerance** (mm)	**Dimension** (mm)	**Value** (mm)	**Tolerance** (mm)
A0	3.35	±0.10	K0	1.10	±0.10
B0	6.35	±0.10	P0	4.00	±0.10
D0	1.50	+0.10/-0.00	P1	8.00	±0.10
D1	1.50	+0.10/-0.00	P2	2.00	±0.05
E	1.75	±0.10	T	0.30	±0.05
F	5.50	±0.05	W	12.00	±0.30

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