T-46-19-11

ACT™ 1 Field Programmable Gate Arrays

Features

- Up to 2000 Gate Array Gates (6000 PLD/LCA™ equivalent gates)
- Replaces up to 53 TTL Packages
- Replaces up to 17 20-Pin PAL™ Packages
- Design Library with over 250 Functions
- Gate Array Architecture Allows Completely Automatic Place and Route
- Up to 547 Programmable Logic Modules
- Up to 273 Flip-Flops
- Flip-Flop Toggle Rates to 100 MHz
- Two In-Circuit Diagnostic Probe Pins Support Speed Analysis to 50 MHz
- Built-In High Speed Clock Distribution Network
- I/O Drive to 4 mA
- Nonvolatile, User Programmable
- Logic Fully Tested Prior to Shipment

Product Family Profile

Device	A1010A	A1020A
Capacity		
Gate Array Equivalent Gates	1200	2000
PLD/LCA Equivalent Gates	3000	6000
TTL Equivalent Packages	34	53
20-Pin PAL Equivalent Packages	12	17
Logic Modules	295	547
Flip-Flops (maximum)	147	273
Routing Resources		
Horizontal Tracks/Channel	22	22
Vertical Tracks/Column	13	13
PLICE Antifuse Elements	112,000	186,000
User I/Os (maximum)	57	69
Packages	44 PLCC	44 PLCC
	68 PLCC	68 PLCC
		84 PLCC
	100 PQFP	100 PQFP
	44 JQCC	44 JQCC
	68 JQCC	68 JQCC
		84 JQCC
		84 CQFP
	84 CPGA	84 CPGA
Performance		
Flip-Flop Toggle Rate (maximum)	95 MHz	95 MHz
System Speed (maximum)	40 MHz	40 MHz
CMOS Process	1.2 µm	1.2 µm

Note:
1. See Product Plan on pages 1-6 for package availability.

Description

The ACT™ 1 family of field programmable gate arrays (FPGAs) offers a variety of package, speed, and application combinations. Devices are implemented in silicon gate, 1.2-micron or 2-micron two-level metal CMOS, and they employ Actel's PLICE™ antifuse technology. The unique architecture offers gate array flexibility, high performance, and instant turnaround through user programming. Device utilization is typically 95% of available logic modules.

ACT 1 devices also provide system designers with unique on-chip diagnostic probe capabilities, allowing convenient testing and debugging. Additional features include an on-chip clock driver with a hardwired distribution network. The network provides efficient clock distribution with minimum skew.

The user-definable I/Os are capable of driving at both TTL and CMOS drive levels. Available packages include plastic and ceramic J-leaded chip carriers, ceramic and plastic quad flatpacks, and ceramic pin grid array.

A security fuse may be programmed to disable all further programming and to protect the design from being copied or reverse engineered.

The Action Logic System

The ACT 1 device family is supported by Actel's Action Logic™ System (ALS), allowing logic design implementation with minimum effort. The ALS interfaces with the resident CAE system to provide a complete gate array design environment: schematic capture, simulation, fully automatic place and route, timing verification, and device programming. The Action Logic System is available for 386™ PC and for Apollo™ and Sun™ workstations and for running Viewlogic®, Mentor Graphics®, Valid™, and OrCAD™.

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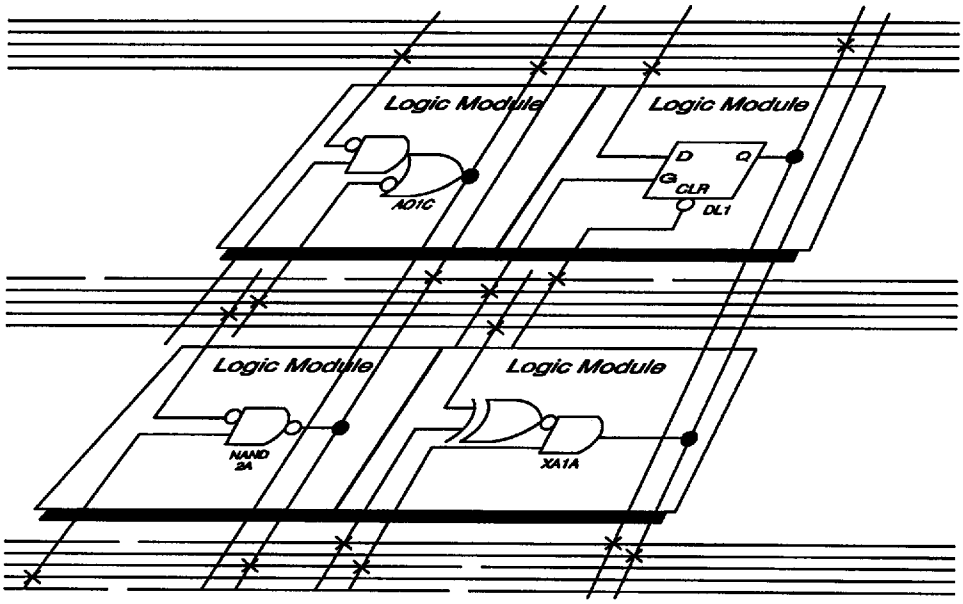


Figure 1. Partial View of an ACT 1 Device

ACT 1 Device Structure

A partial view of an ACT 1 device (Figure 1) depicts four logic modules and distributed horizontal and vertical interconnect tracks. PLICE antifuses, located at intersections of the horizontal and vertical tracks, connect logic module inputs and outputs. During programming, these antifuses are addressed and programmed to make the connections required by the circuit application.

The Actel Logic Module

The Actel logic module is an 8-input, one-output logic circuit chosen for the wide range of functions it implements and for its efficient use of interconnect routing resources (Figure 2).

The logic module can implement the four basic logic functions (NAND, AND, OR, and NOR) in gates of two, three, or four inputs. Each function may have many versions, with different combinations of active-low inputs. The logic module can also implement a variety of D-latches, exclusivity function, AND-ORs, and OR-ANDs. No dedicated hardwired latches or flip-flops are required in the array since latches and flip-flops may be constructed from logic modules wherever needed in the application.

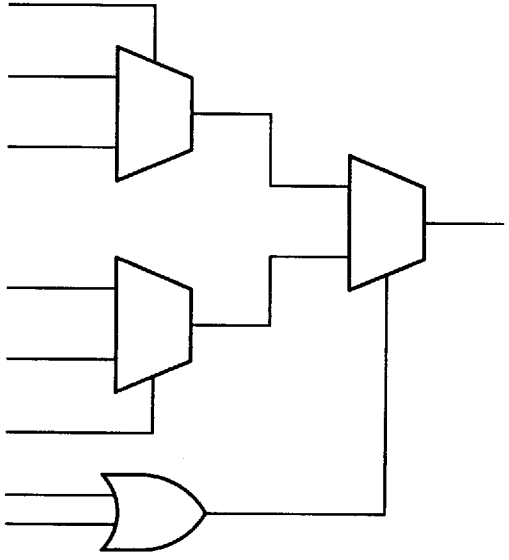


Figure 2. ACT 1 Logic Module

I/O Buffers

Each I/O pin is available as an input, output, three-state, or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Outputs sink or source 4 mA at TTL levels. See Electrical Specifications for additional I/O buffer specifications.

Device Organization

ACT 1 devices consist of a matrix of logic modules arranged in rows separated by wiring channels. This array is surrounded by a ring of peripheral circuits including I/O buffers, testability circuits, and diagnostic probe circuits providing real-time diagnostic capability. Between rows of logic modules are routing channels containing sets of segmented metal tracks with PLICE antifuses. Each channel has 22 signal tracks. Vertical routing is permitted via 13 vertical tracks per logic module column. The resulting network allows arbitrary and flexible interconnections between logic modules and I/O modules.

Probe Pin

ACT 1 devices have two independent diagnostic probe pins. These pins allow the user to observe any two internal signals by entering the appropriate net name in the diagnostic software. Signals may be viewed on a logic analyzer using Actel's Actionprobe™ diagnostic tools. The probe pins can also be used as user-defined I/Os when debugging is finished.

ACT 1 Array Performance T-46-19-11

Temperature and Voltage Effects

Worst-case delays for ACT 1 arrays are calculated in the same manner as for masked array products. A typical delay parameter is multiplied by a derating factor to account for temperature, voltage, and processing effects. However, in an ACT 1 array, temperature and voltage effects are less dramatic than with masked devices. The electrical characteristics of module interconnections on ACT 1 devices remain constant over voltage and temperature fluctuations.

As a result, the total derating factor from typical to worst case for a standard speed ACT 1 array is only 1.19 to 1, compared to 2 to 1 for a masked gate array.

Logic Module Size

Logic module size also affects performance. A mask programmed gate array cell with four transistors usually implements only one logic level. In the more complex logic module (similar to the complexity of a gate array macro) of an ACT 1 array, implementation of multiple logic levels within a single module is possible. This eliminates interlevel wiring and associated RC delays. The effect is termed "net compression."

1

Ordering Information

A1010 A – 2 PL 84 C

- C — Application (Temperature Range)
  - C = Commercial (0 to +75°C)
  - I = Industrial (–40 to +85°C)
  - M = Military (–55 to +125°C)
  - B = MIL-STD-883
  - E = Extended Flow
- 84 — Package Lead Count
- PL — Package Type
  - PL = Plastic J-Leaded Chip Carriers
  - PQ = Plastic Quad Flatpacks
  - CQ = Ceramic Quad Flatpack
  - JQ = J-leaded Cerquad Chip Carrier
  - PG = Ceramic Pin Grid Array
- 2 — Speed Grade
  - Std = Standard Speed
  - –1 = Standard + 15% Speed
  - –2 = Standard + 25% Speed
- A — Die Revision
- A1010 — Part Number
  - A1010A = 1200 Gates
  - A1020A = 2000 Gates

T-46-19-11

Product Plan

	Speed Grade*			Application				
	Std	–1	–2	C	I	M	B	E
A1010A Device								
44-pin Plastic Leaded Chip Carrier (PL)	✓	✓	✓	✓	✓	–	–	–
68-pin Plastic Leaded Chip Carrier (PL)	✓	✓	✓	✓	✓	–	–	–
100-pin Plastic Quad Flatpack (PQ)	✓	✓	✓	✓	✓	–	–	–
84-pin Ceramic Pin Grid Array (PG)	✓	✓	–	✓	–	✓	✓	–
A1020A Device								
44-pin Plastic Leaded Chip Carrier (PL)	✓	✓	✓	✓	✓	–	–	–
68-pin Plastic Leaded Chip Carrier (PL)	✓	✓	✓	✓	✓	–	–	–
84-pin Plastic Leaded Chip Carrier (PL)	✓	✓	✓	✓	✓	–	–	–
100-pin Plastic Quad Flatpack (PQ)	✓	✓	✓	✓	✓	–	–	–
84-pin Ceramic Pin Grid Array (PG)	✓	✓	–	✓	–	✓	✓	–
84-pin Ceramic Quad Flatpack (CQ)	✓	✓	–	✓	–	✓	✓	✓
44-pin J-leaded Cerquad Chip Carrier (JQ)	✓	✓	–	✓	–	✓	✓	–
68-pin J-leaded Cerquad Chip Carrier (JQ)	✓	✓	–	✓	–	✓	✓	–
84-pin J-leaded Cerquad Chip Carrier (JQ)	✓	✓	–	✓	–	✓	✓	–

Applications: C = Commercial, I = Industrial, M = Military, B = MIL-STD-883, E = Extended Flow

Availability: ✓ = Available, P = Planned, – = Not Planned

* Speed Grade: –1 = 15% faster than Standard, –2 = 25% faster than Standard

Device Resources

Device Series	Logic Modules	Gates	User I/Os			
			44-pin	68-pin	84-pin	100-pin
A1010A	295	1200	34	57	57	57
A1020A	547	2000	34	57	69	69

T-46-19-11

Pin Description

CLK Clock (Input)

TTL Clock input for global clock distribution network. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

DCLK Diagnostic Clock (Input)

TTL Clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

GND Ground (Input)

Input LOW supply voltage.

I/O Input/Output (Input, Output)

I/O pin functions as an input, output, three-state, or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/O pins are automatically driven LOW by the ALS software.

MODE Mode (Input)

The MODE pin controls the use of multi-function pins (DCLK, PRA, PRB, SDI). When the MODE pin is HIGH, the special functions are active. When the MODE pin is LOW, the pins function as I/O.

NC No Connection

This pin is not connected to circuitry within the device.

$\overline{PRA}$ Probe A (Output)

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin is used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect the programmed designs confidentiality. PRA is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

$\overline{PRB}$ Probe B (Output)

The Probe B pin is used to output data from any user-defined design node within the device. This independent diagnostic pin is used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect the programmed design's confidentiality. PRB is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

SDI Serial Data Input (Input)

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

V_{CC} Supply Voltage (Input)

Input HIGH supply voltage.

V_{PP} Programming Voltage (Input)

Input supply voltage used for device programming. This pin must be connected to V_{CC} during normal operation.

Absolute Maximum Ratings

Free air temperature range

Symbol	Parameter	Limits	Units
V_{CC}	DC Supply Voltage[1]	-0.5 to +7.0	Volts
V_I	Input Voltage	-0.5 to V_{CC} +0.5	Volts
V_O	Output Voltage	-0.5 to V_{CC} +0.5	Volts
I_{IK}	Input Clamp Current	±20	mA
I_{OK}	Output Clamp Current	±20	mA
I_{OK}	Continuous Output Current	±25	mA
T_{STG}	Storage Temperature	-65 to +150	°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the Recommended Operating Conditions.

Note:

1. $V_{PP} = V_{CC}$, except during device programming.

Recommended Operating Conditions

Parameter	Commercial	Industrial	Military	Units
Temperature Range[1]	0 to +70	-40 to +85	-55 to +125	°C
Power Supply Tolerance	±5	±10	±10	%V_{CC}

Note:

1. Ambient temperature (T_A) used for commercial and industrial; case temperature (T_C) used for military.

Electrical Specifications

Parameter		Commercial		Industrial		Military		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}[1]	(I_{OH} = -4 mA)	3.84						V
	(I_{OH} = -3.2 mA)			3.7		3.7		V
V_{OL}[1]	(I_{OL} = 4 mA)		0.33		0.40		0.40	V
V_{IL}		-0.3	0.8	-0.3	0.8	-0.3	0.8	V
V_{IH}		2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
Input Transition Time t_R, t_F[2]			500		500		500	ns
C_{IO} I/O Capacitance[2, 3]			10		10		10	pF
Standby Current, I_{CC}[4]			10		20		25	mA
Leakage Current[5]		-10	10	-10	10	-10	10	µA
I_{OS} Output Short Circuit Current[6]	(V_O = V_{CC})	20	140	20	140	20	140	mA
	(V_O = GND)	-10	-100	-10	-100	-10	-100	mA

Notes:

1. Only one output tested at a time. V_{CC} = min.
2. Not tested, for information only.
3. Includes worst-case 84-pin PLCC package capacitance. V_{OUT} = 0 V, f = 1 MHz.
4. Typical standby current = 3 mA. All outputs unloaded. All inputs = V_{CC} or GND.
5. V_O, V_{IN} = V_{CC} or GND.
6. Only one output tested at a time. Min. at V_{CC} = 4.5 V; Max. at V_{CC} = 5.5 V.

Package Thermal Characteristics

The device junction to case thermal characteristic is θjc, and the junction to ambient air characteristic is θja. The thermal characteristics for θja are shown with two different air flow rates.

Maximum junction temperature is 150°C.

A sample calculation of the maximum power dissipation for an 84-pin plastic leaded chip carrier at commercial temperature is as follows:

T-46-19-11

$$\frac{\text{Max. junction temp. (°C)} - \text{Max. commercial temp. (°C)}}{\text{θja (°C/W)}} = \frac{150°C - 70°C}{44°C/W} = 1.82\ W$$

Package Type	Pin Count	θjc	θja Still air	θja 300 ft/min.	Units
Plastic J-leaded Chip Carrier	44	15	52	40	°C/W
	68	13	45	35	°C/W
	84	12	44	33	°C/W
Plastic Quad Flatpack	100	13	55	47	°C/W
Ceramic Pin Grid Array	84	8	33	20	°C/W
Ceramic Quad Flatpack	84	5	40	30	°C/W
J-leaded Cerquad Chip Carrier	44	8	38	30	°C/W
	68	8	35	25	°C/W
	84	8	34	24	°C/W

Power Dissipation

The following formula is used to calculate total device dissipation.

Total Device Power (mW) = (0.20 x N x F1) + (0.085 x M x F2) + (0.80 x P x F3)

Where:

F1 = Average logic module switching rate in MHz

F2 = CLKBUF macro switching rate in MHz

F3 = Average I/O module switching rate in MHz

M = Number of logic modules connected to the CLKBUF macro

N = Total number of logic modules used in the design (including M)

P = Number of outputs loaded with 50 pF

Average switching rate of logic modules and of I/O modules is some fraction of the device operating frequency (usually CLKBUF). Logic modules and I/O modules switch states (from low-to-high or from high-to-low) only if the input data changes when the module is enabled. A conservative estimate for average logic module and I/O module switching rates (variables F1 and F3, respectively) is 10% of device clock driver frequency.

If the CLKBUF macro is not used in the design, eliminate the second term (including F2 and M variables) from the formula.

Sample A1020 Device Power Calculation

To illustrate the power calculation, consider a large design operating at high frequency. This sample design utilizes 85% of available logic modules on the A1020-series device (.85 x 547 = 465 logic modules used). The design contains 104 flip-flops (208 logic modules). Operating frequency of the design is 16 MHz. In this design, the CLKBUF macro drives the clock network. Logic modules and I/O modules are switching states at approximately 10% of the clock frequency rate (.10 x 16 MHz = 1.6 MHz). Sixteen outputs are loaded with 50 pF.

To summarize the design described above: N = 464; M = 208; F2 = 16; F1 = 4; F3 = 4; P = 16. Total device power can be calculated by substituting these values for variables in the device dissipation formula.

Total device power for this example =

(0.20 x 465 x 1.6) + (0.085 x 208 x 16) + (0.80 x 16 x 1.6) = 452 mW

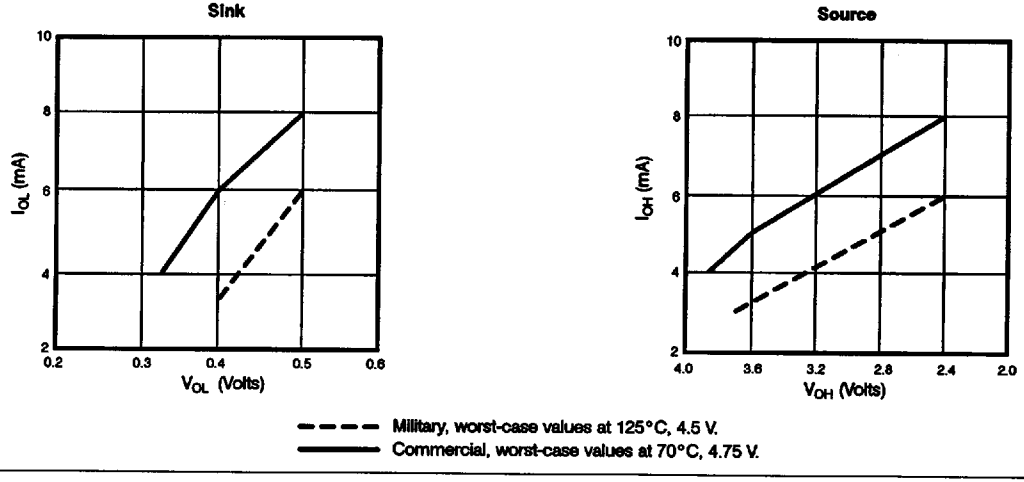
Functional Timing Tests

AC timing for logic module internal delays is determined after place and route. The ALS Timer utility displays actual timing parameters for circuit delays. ACT 1 devices are AC tested to a "binning" circuit specification.

The circuit consists of one input buffer + n logic modules + one output buffer (n=16 for A1010A; n=28 for A1020A). The logic modules are distributed along two sides of the device, as inverting or non-inverting buffers. The modules are connected through programmed antifuses with typical capacitive loading.

Propagation delay [$t_{PD} = (t_{PLH} + t_{PHL})/2$] is tested to the following AC test specifications.

Output Buffer Performance Derating



Note:
The above curves are based on characterizations of sample devices and are not completely tested on all devices.

T-46-19-11

Timing Derating

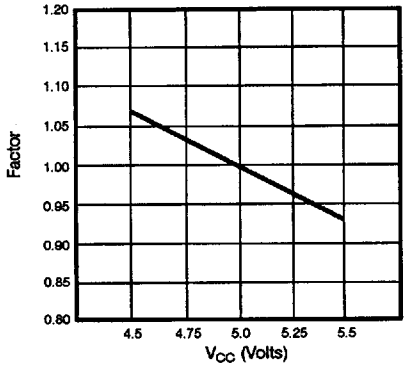
Operating temperature, operating voltage, and device processing conditions, along with device die size and speed grade, account for variations in array timing characteristics. These variations are summarized into a derating factor for ACT 1 array typical timing specifications. The derating factors shown in the table below are based on the recommended operating conditions for ACT 1 commercial, industrial, and military applications. The derating curves show worst-to-best case operating voltage range and best-to-worst case operating temperature range.

Timing Derating Factor (x typical)

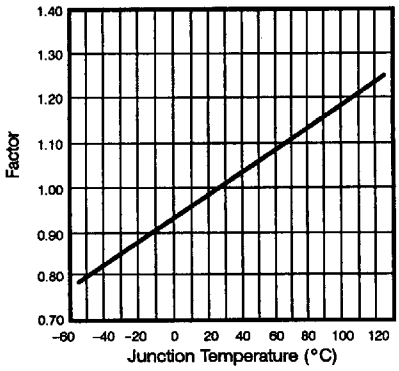
	Commercial		Industrial		Military	
Device	**Best-Case**	**Worst-Case**	**Best-Case**	**Worst-Case**	**Best-Case**	**Worst-Case**
A1010A, A1020A						
Standard Speed	0.45	1.54	0.40	1.65	0.37	1.79
–1 Speed Grade	0.45	1.28	0.40	1.37	0.37	1.49
–2 Speed Grade	0.45	1.13	0.40	1.20	0.37	1.32

Note:
"Best-case" reflects maximum operating voltage, minimum operating temperature, and best-case processing. "Worst-case" reflects minimum operating voltage, maximum operating temperature, and worst-case processing. Best-case derating is based on sample data only and is not guaranteed.

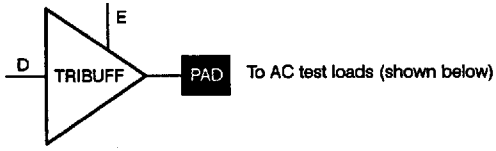
Voltage Derating Curve

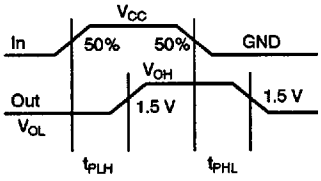


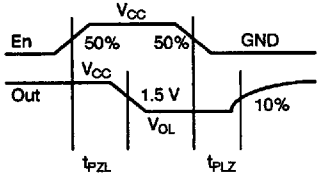
Temperature Derating Curve

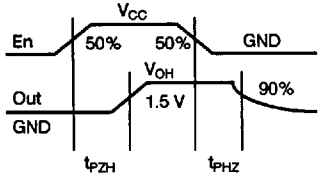


Output Buffer Delays



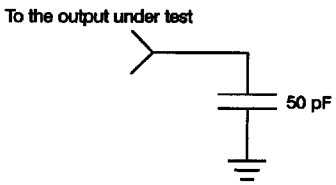




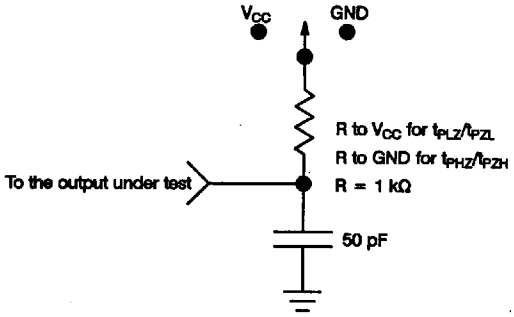


AC Test Loads

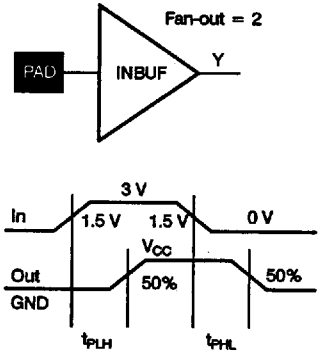
Load 1
(Used to measure propagation delay)



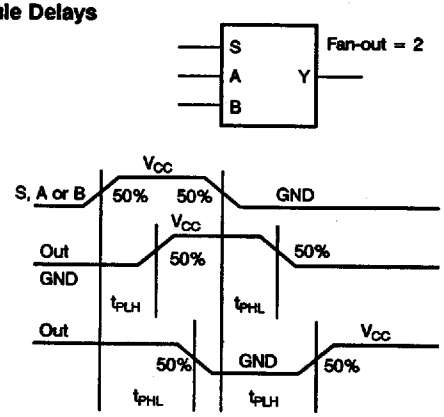
Load 2
(Used to measure rising/falling edges)



Input Buffer Delays

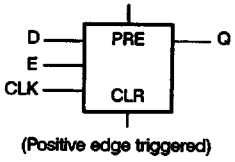


Module Delays

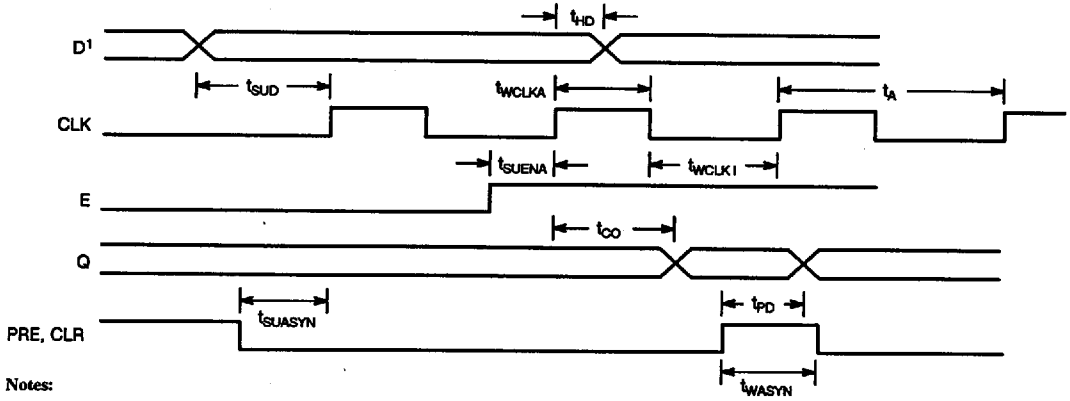


Sequential Timing Characteristics

Flip-Flops and Latches



(Positive edge triggered)



Notes:

1. D represents all data functions involving A, B, and S for multiplexed flip-flops.

T-46-19-11

Timing Characteristics

Timing is design-dependent; actual delay values are determined after place and route of the design using the ALS Timer utility. The following delay values use statistical estimates for wiring delays based on 85% to 90% module utilization. Device utilization above 95% will result in performance degradation.

With ALS place and route programs, the user can assign criticality level to a net, based on timing requirements. Delays for both typical and critical (speed-sensitive) nets are given below. Most nets will fall into the "typical" category.

Less than 1% of all routing in a design requires the use of "long tracks." Long tracks, long vertical or horizontal routing paths, are used by the autorouter only as needed. Delays due to the use of long tracks range from 15 ns to 35 ns. Long tracks may be used to route the least critical nets in a given design.

Logic Module Timing

V_{CC} = 5.0 V; T_J = 25°C; Process = Typical; t_{PD} = 3.0 ns @ FO = 0

Single Logic Module Macros (e.g., most gates, latches, multiplexors)[1]

Parameter	Output Net	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	Units
t_{PD}	Critical	5.4	5.8	6.2	8.5	Note 2	ns
t_{PD}	Typical	6.3	6.7	7.7	8.6	10.8	ns

Dual Logic Module Macros (e.g., adders, wide input gates)[1]

Parameter	Output Net	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	Units
t_{PD}	Critical	9.2	9.6	10.0	12.3	Note 2	ns
t_{PD}	Typical	10.2	10.6	11.6	12.5	14.6	ns

Sequential Element Timing Characteristics

Parameter		Fan-Out					Units
		FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	
t_{SU}	Set Up Time, Data Latches	3.5	3.9	4.2	4.5	4.8	ns
t_{SU}	Set Up Time, Flip-Flops	3.9	3.9	3.9	3.9	3.9	ns
t_H	Hold Time	0	0	0	0	0	ns
t_W	Pulse Width, Minimum[3]	7.7	8.5	9.2	10.0	14.0	ns
t_{CO}	Delay, Critical Net	5.4	5.8	6.2	8.5	Note 2	ns
t_{CO}	Delay, Typical Net	6.3	6.7	7.7	8.6	10.8	ns

Notes:

1. Most flip-flops exhibit single module delays.
2. Critical nets have a maximum fan-out of six.
3. Minimum pulse width, t_W, applies to CLK, PRE, and CLR inputs.

T-46-19-11

I/O Buffer Timing

V_{CC} = 5.0 V; T_J = 25°C; Process = Typical

INBUF Macros

Parameter	From – To	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	Units
t_{PHL}	Pad to Y	6.9	7.6	8.9	10.7	14.3	ns
t_{PLH}	Pad to Y	5.9	6.5	7.7	8.4	12.4	ns

CLKBUF (High Fan-Out Clock Buffer) Macros

Parameter	FO = 40	FO = 160	FO = 320	Units
t_{PHL}	9.0	12.0	15.0	ns
t_{PLH}	9.0	12.0	15.0	ns

Notes:

1. A clock balancing feature is provided to minimize clock skew.
2. There is no limit to the number of loads that may be connected to the CLKBUF macro.

OUTBUF, TRIBUFF, and BIBUF Macros[1]

C_L = 50 pF

Parameter	From – To	CMOS	TTL	Units
t_{PHL}	D to Pad	3.9	4.9	ns
t_{PLH}	D to Pad	7.2	5.7	ns
t_{PHZ}	E to Pad	5.2	3.4	ns
t_{PZH}	E to Pad	6.5	4.9	ns
t_{PLZ}	E to Pad	6.9	5.2	ns
t_{PZL}	E to Pad	4.9	5.9	ns

Change in Propagation Delay with Load Capacitance[2]

Parameter	From – To	CMOS	TTL	Units
t_{PHL}	D to Pad	0.03	0.046	ns/pF
t_{PLH}	D to Pad	0.07	0.039	ns/pF
t_{PHZ}	E to Pad	0.06	0.046	ns/pF
t_{PZH}	E to Pad	0.07	0.039	ns/pF
t_{PLZ}	E to Pad	0.07	0.039	ns/pF
t_{PZL}	E to Pad	0.03	0.039	ns/pF

Notes:

1. The BIBUF macro input section exhibits the same delays as the INBUF macro.
2. Load capacitance delay delta can be extrapolated down to 15 pF minimum.

   Example:

   Delay for OUTBUF driving a 100-pF TTL load:

   t_{PHL} = 4.9 + (.046 x (100–50)) = 4.9 + 2.3 = 7.2 ns

   t_{PLH} = 5.7 + (.039 x (100–50)) = 5.7 + 2.0 = 7.7 ns

T-46-19-11

Soft Macro Library Overview

Macro Name	Modules Required	Description	Levels of Logic
Counters			
CNT4A	17	4-bit loadable binary counter with clear	4
CNT4B	15	4-bit loadable bin counter w/ clr, active low carry in & carry out	4
UDCNT4A	24	4-bit up/down cntr w/ sync active low load, carry in & carry out	6
Decoders			
DEC2X4	4	2 to 4 decoder	1
DEC2X4A	4	2 to 4 decoder with active low outputs	1
DEC3X8	8	3 to 8 decoder	1
DEC3X8A	8	3 to 8 decoder with active low outputs	1
DEC4X16A	20	4 to 16 decoder with active low outputs	2
DECE2X4	4	2 to 4 decoder with enable	1
DECE2X4A	4	2 to 4 decoder with enable and active low outputs	1
DECE3X8	11	3 to 8 decoder with enable	2
DECE3X8A	11	3 to 8 decoder with enable and active low outputs	2
Latches and Registers			
DLC8A	8	Octal latch with clear	1
DLE8	8	Octal latch with enable	1
DLM8	8	Octal latch with mulitplexed inputs	1
REGE8A	20	Octal register with preset and clear, active high enable	2
REGE8B	20	Octal register with active low clock, preset and clear, active high enable	2
Adders			
FA1	3	One bit full adder	3
FADD8	37	8-bit fast adder	4
FADD12	62	12-bit fast adder	5
FADD16	78	16-bit fast adder	5
FADD24	120	24-bit fast adder	6
FADD32	160	32-bit fast adder	7
Comparators			
ICMP4	5	4-bit identity comparator	2
ICMP8	9	8-bit identity comparator	3
MCMP16	93	16-bit magnitude comparator	5
MCMPC2	9	2-bit magnitude comparator with enables	3
MCMPC4	18	4-bit magnitude comparator with enables	4
MCMPC8	36	8-bit magnitude comparator with enables	6
Multiplexors			
MX8	3	8 to 1 multiplexor	2
MX8A	3	8 to 1 multiplexor with an active low output	2
MX16	5	16 to 1 multiplexor	2
Multipliers			
SMULT8	235	8 x 8 two's complement multiplier	Varies

1

Soft Macro Library Overview (continued)

T-46-19-11

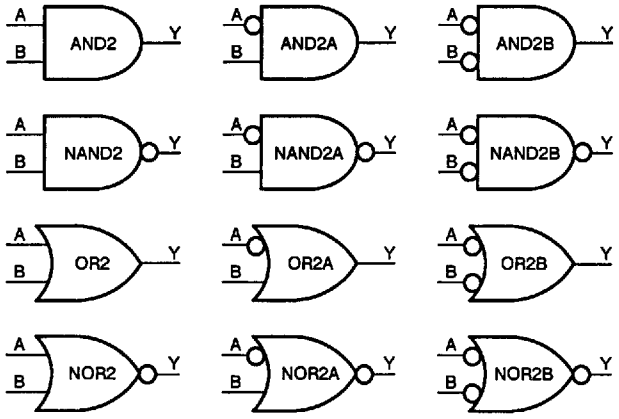
Macro Name	Modules Required	Description	Levels of Logic
Shift Registers			
SREG4A	8	4-bit shift register with clear	2
SREG8A	18	8-bit shift register with clear	2
TTL Replacements			
TA138	12	3 to 8 decoder with 3 enables and active low outputs	2
TA139	4	2 to 4 decoder with an enable and active low outputs	1
TA151	5	8 to 1 multiplexor with enable, true, and complementary outputs	3
TA153	2	4 to 1 multiplexor with active low enable	2
TA157	1	2 to 1 multiplexor with enable	1
TA161	22	4-bit sync counter w/ load, clear, count enables & ripple carry out	3
TA164	18	8-bit serial in, parallel out shift register	1
TA169	25	4-bit synchronous up / down counter	6
TA181	31	4-bit ALU	4
TA194	14	4-bit shift register	1
TA195	10	4-bit shift register	1
TA269	50	8-bit up/down cntr w/ clear, load, ripple carry output & enables	8
TA273	18	Octal register with clear	1
TA280	9	Parity generator and checker	4
TA377	16	Octal register with active low enable	1
Super Macros			
MC	102	DRAM Controller	Varies
DMA	225	Direct Memory Access Controller	Varies
SINT	180	SCSI Interface Controller	Varies

Hard Macro Library Overview

The following illustrations show all the available Hard Macros.

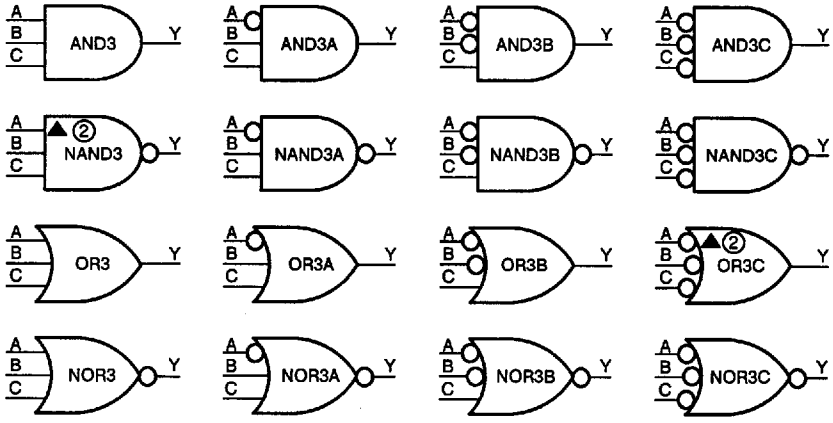
T-46-19-11

2-Input Gates (Module Count = 1)



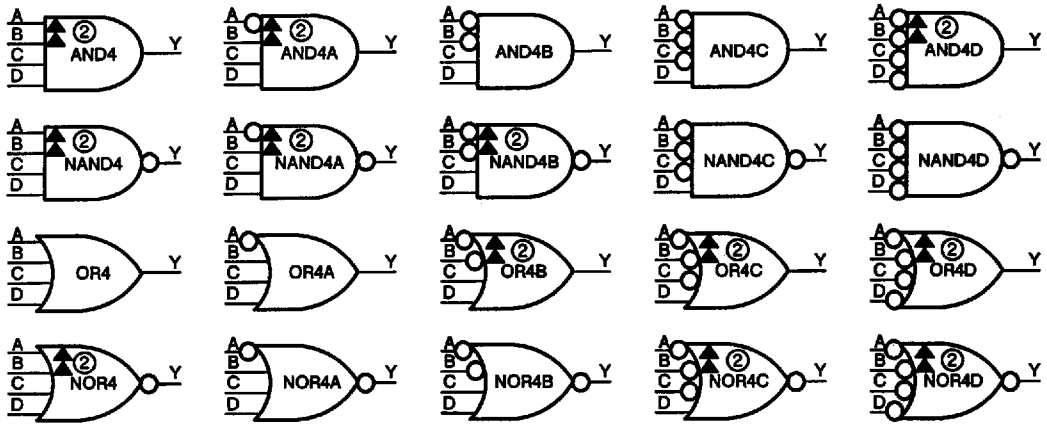
3-Input Gates (Module Count = 1, unless indicated otherwise)

② Indicates 2-module macro
▲ Indicates extra delay input

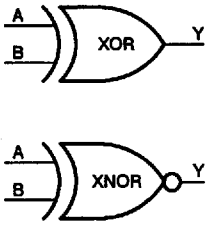


4-Input Gates (Module Count = 1, unless indicated otherwise)

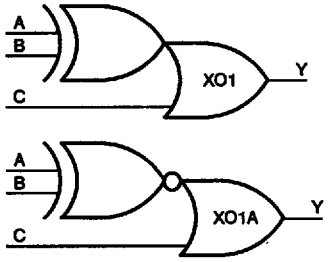
② Indicates 2-module macro
▲ Indicates extra delay input



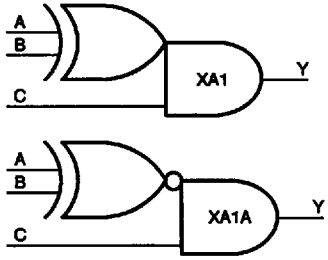
XOR Gates
(Module Count = 1)



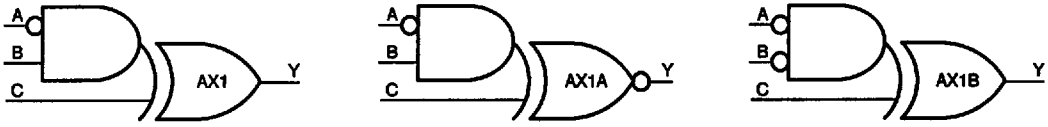
XOR-OR Gates
(Module Count = 1)



XOR-AND Gates
(Module Count = 1)



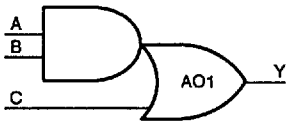
AND-XOR Gates
(Module Count = 1)

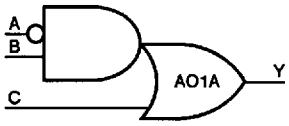


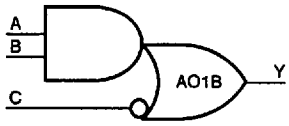
T-46-19-11

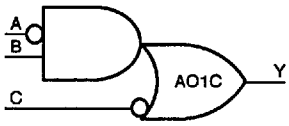
AND-OR Gates (Module Count = 1)

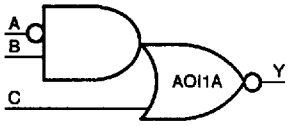
② Indicates 2-module macro
▲ Indicates extra delay input

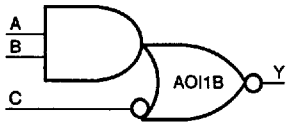


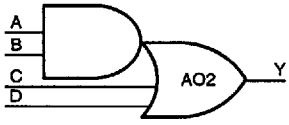


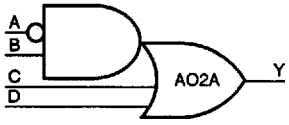


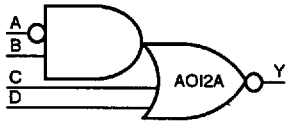


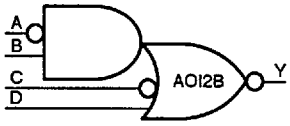


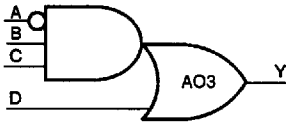


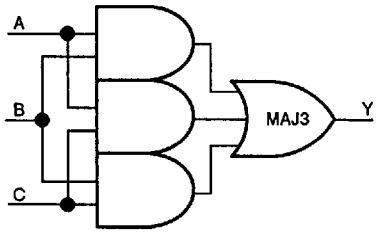


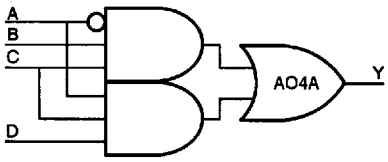


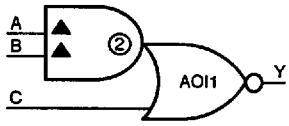


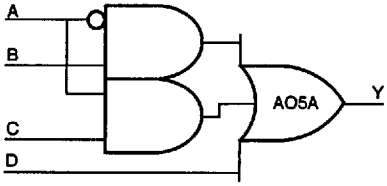


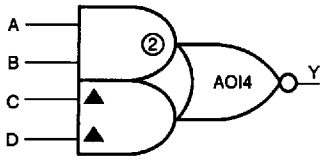


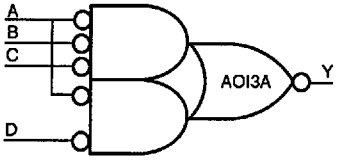








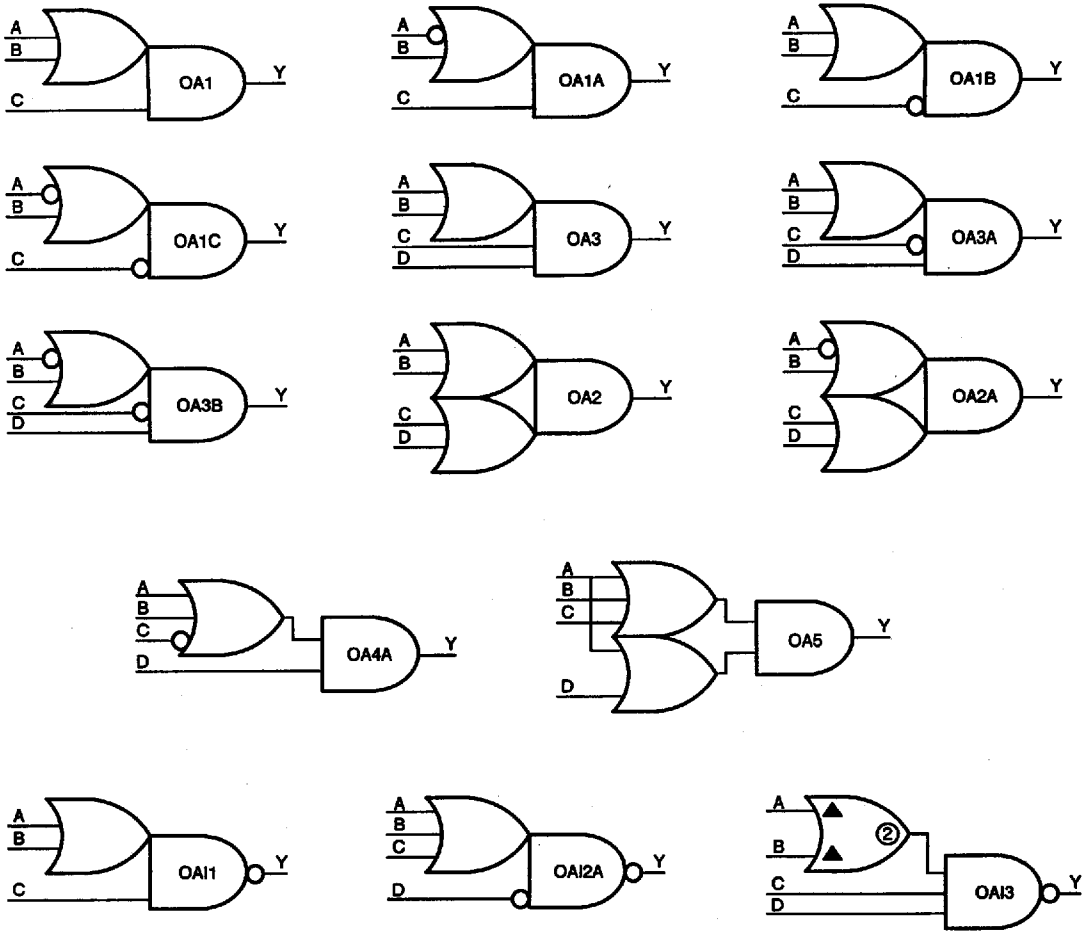




T-46-19-11

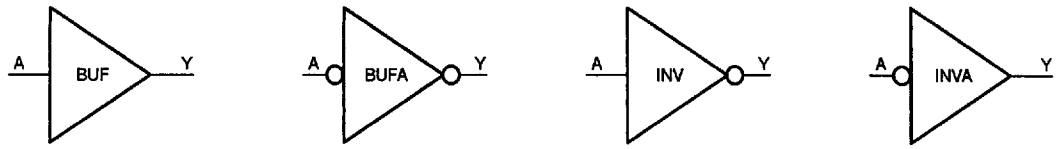
OR-AND Gates (Module Count = 1)

② Indicates 2-module macro
▲ Indicates extra delay input

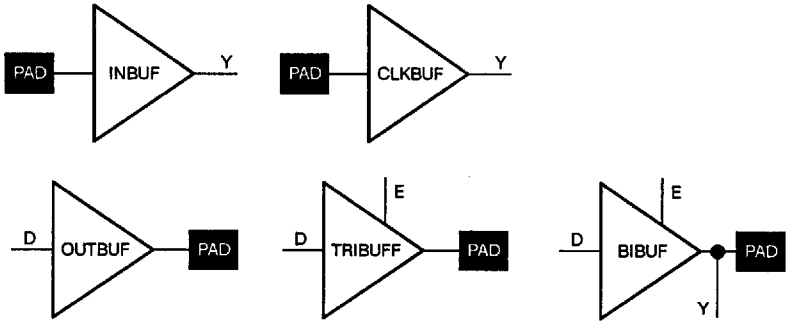


T-46-19-11

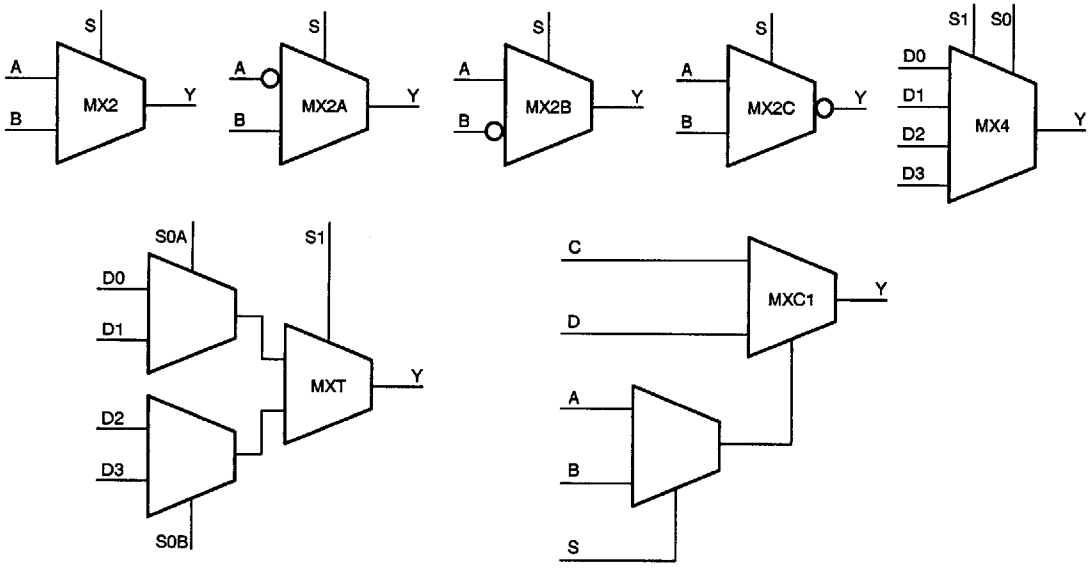
Buffers (Module Count = 1)



I/O Buffers (I/O Module Count = 1)

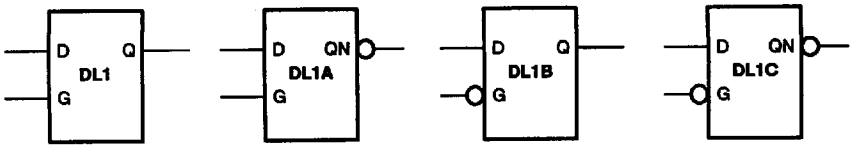


Multiplexors (Module Count = 1)

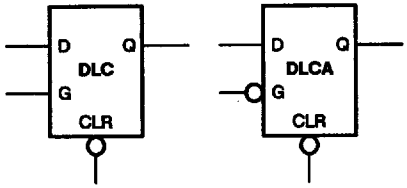


T-46-19-11

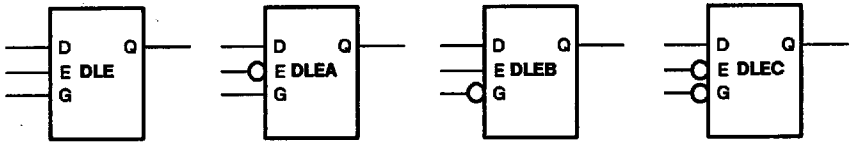
Latches (Module Count = 1)



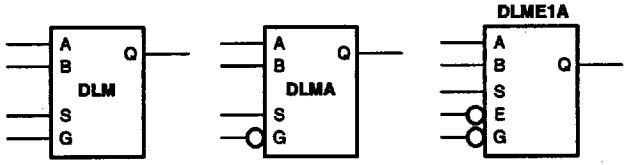
D-Latches with Clear (Module Count = 1)



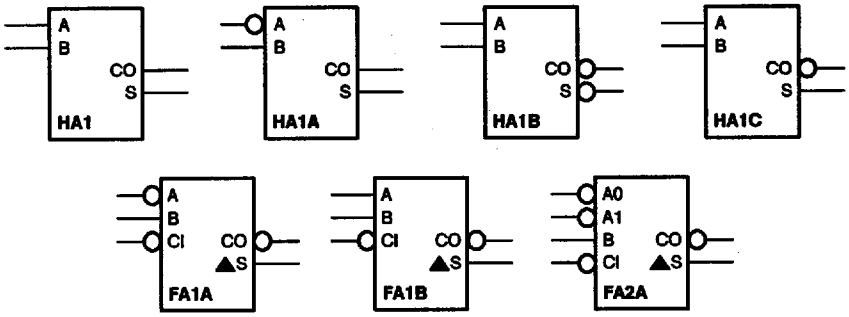
D-Latches with Enable (Module Count = 1)



Mux Latches (Module Count = 1)



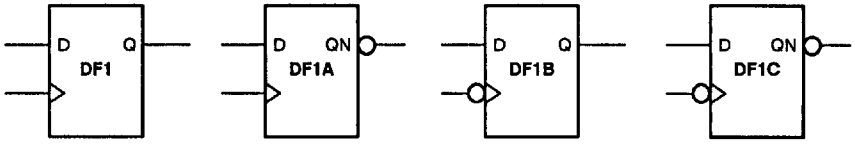
Adders (Module Count = 2)



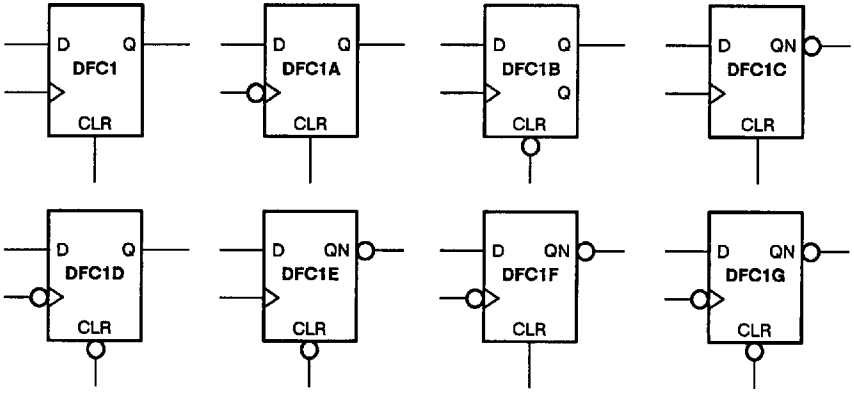
Macros FA1A, FA1B, and FA2A have two level delays from the inputs to the S outputs, as indicated by the▲

T-46-19-11

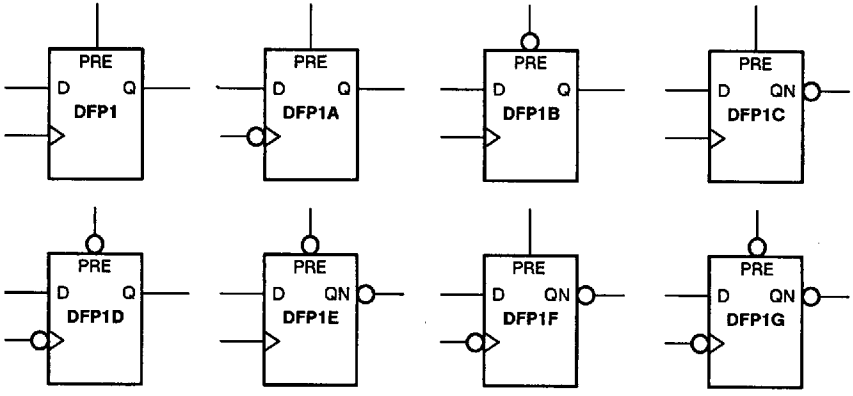
D-Type Flip-Flops (Module Count = 2)



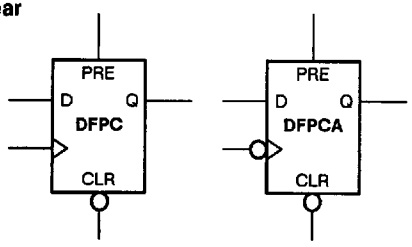
D-Type Flip-Flops with Clear



D-Type Flip-Flops with Preset

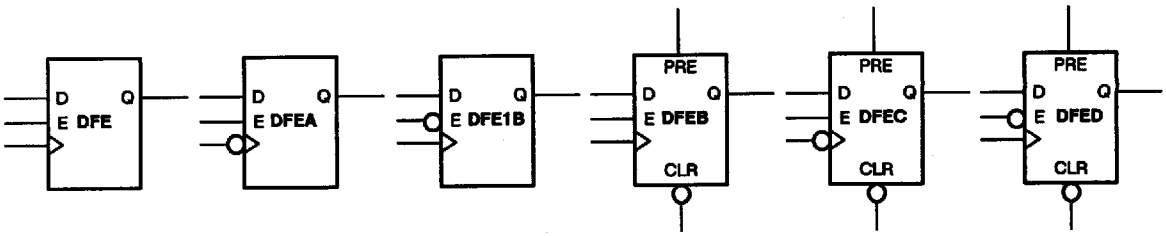


D-Type Flip-Flops with Preset and Clear

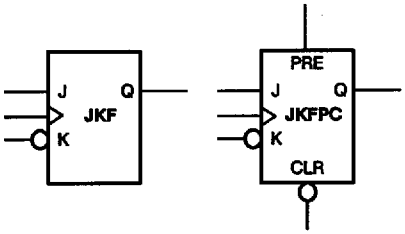


T-46-19-11

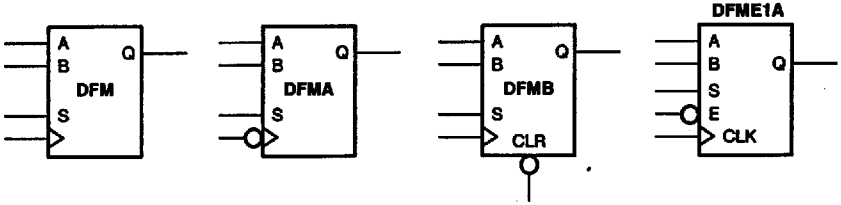
D-Type Flip-Flops with Enable (Module Count = 2)



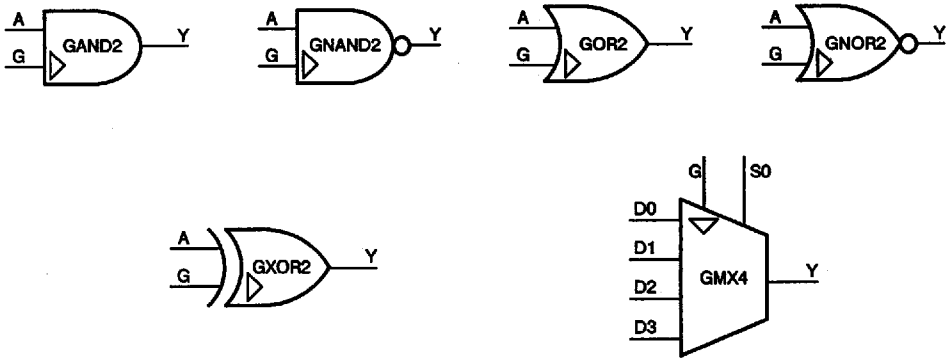
JK Flip-Flops (Module Count = 2)



Mux Flip-Flops (Module Count = 2)

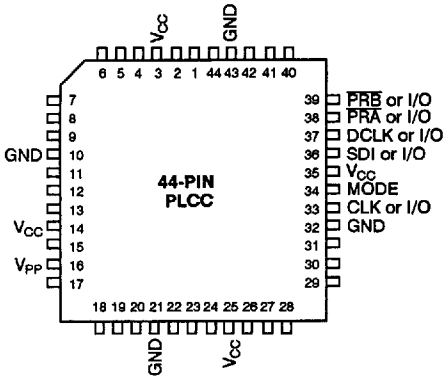


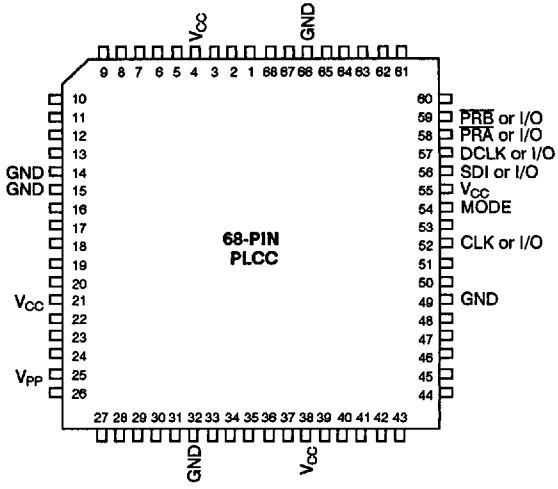
CLKBUF Interface Macros (Module Count = 1)

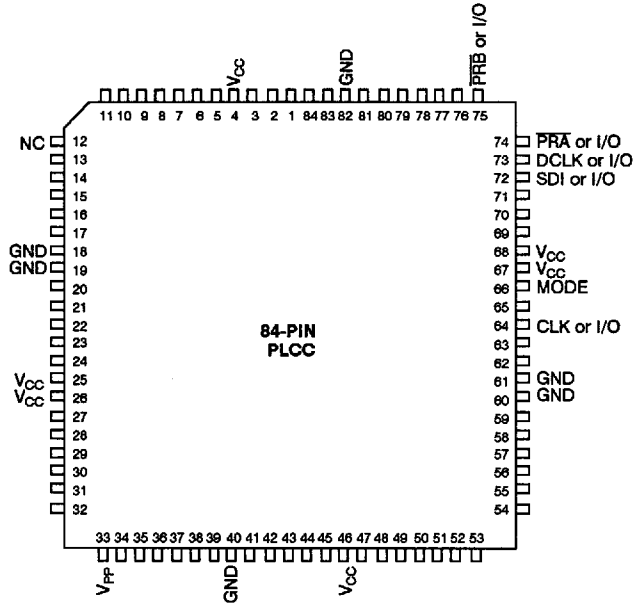


Package Pin Assignments (Top View)

T-46-19-11





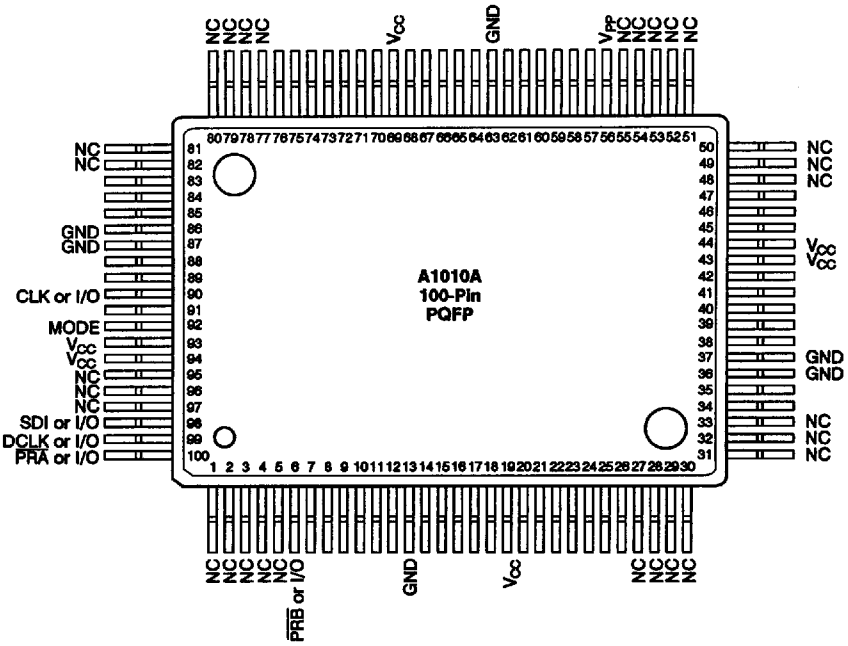


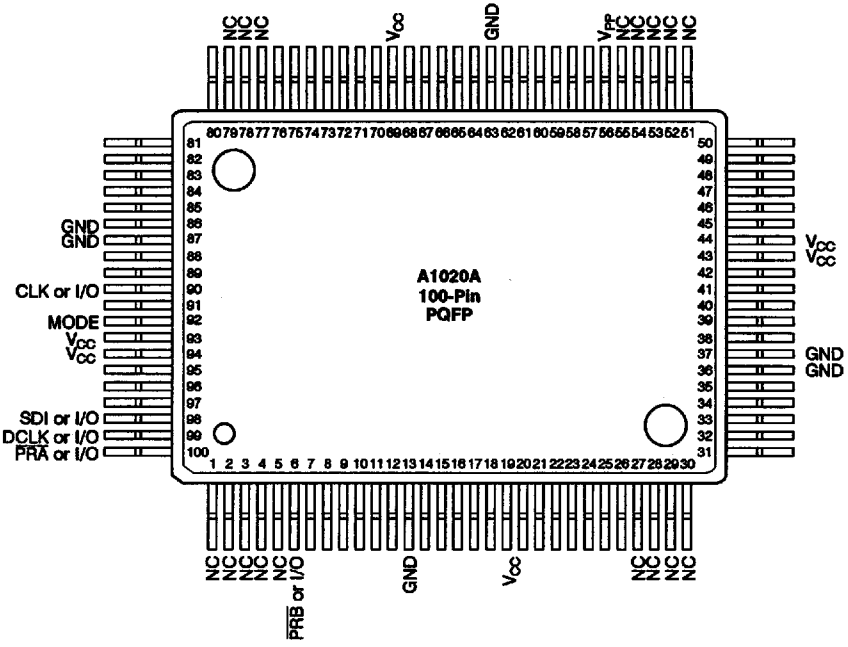
Notes:

1. V_{PP} must be terminated to V_{CC}, except during device programming.
2. MODE must be terminated to circuit ground, except during device programming or debugging.
3. Unused I/O pins are designated as outputs by ALS and are driven low.
4. All unassigned pins are available for use as I/Os.

Package Pin Assignments (continued)
(Top View)

T-46-19-11





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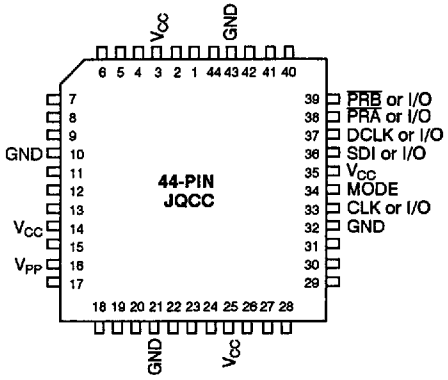
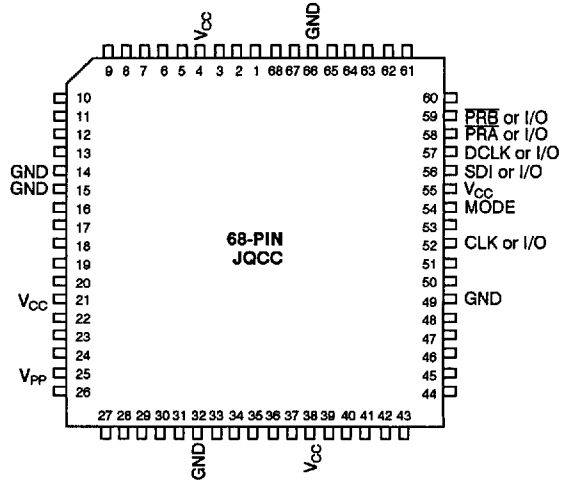
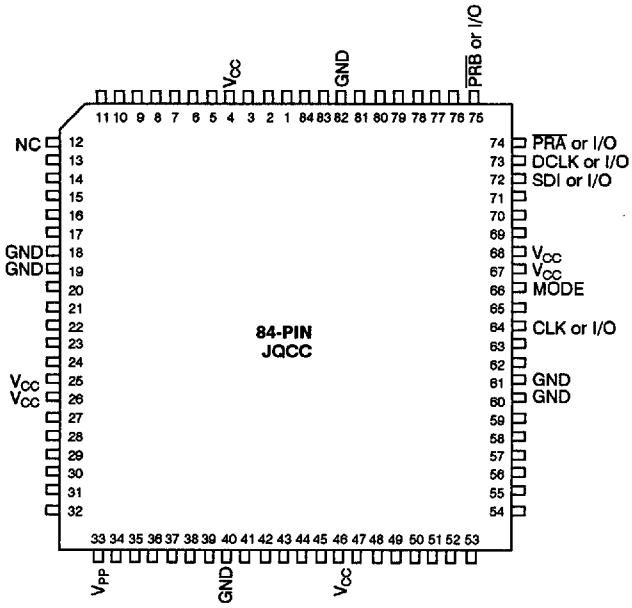
Package Pin Assignments (continued)

T-46-19-11







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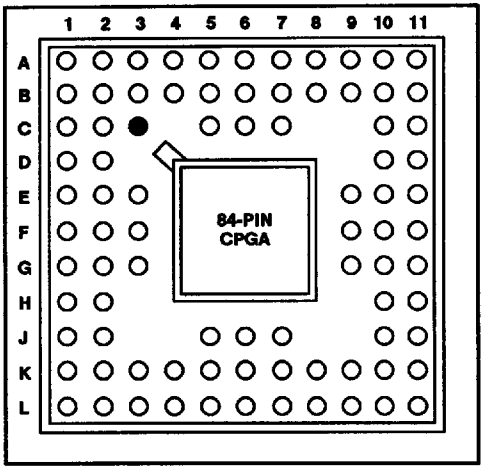
Package Pin Assignments (continued)

T-46-19-11



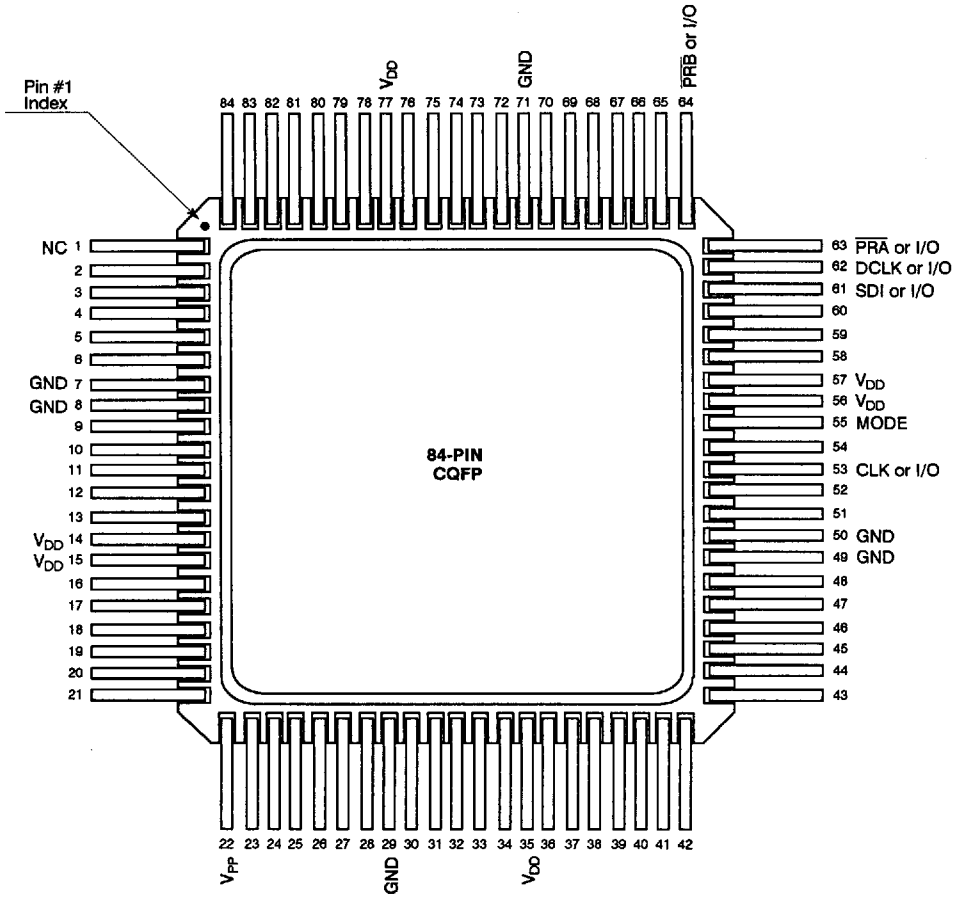
● Orientation Pin (C3)

Signal	A1010-Series Devices	A1020-Series Devices
$\overline{PRA}$	A11	A11
$\overline{PRB}$	B10	B10
MODE	E11	E11
SDI	B11	B11
DCLK	C10	C10
V_{PP}	K2	K2
CLK or I/O	F9	F9
GND	B7, E2, E3, K5, F10, G10	B7, E2, E3, K5, F10, G10
V_{CC}	B5, F1, G2, K7, E9, E10	B5, F1, G2, K7, E9, E10
N/C (No Connection)	B1, B2, C1, C2, K1, J2, L1, J10, K10, K11, C11, D10, D11	B2

Notes:
1. V_{PP} must be terminated to V_{CC}, except during device programming.
2. MODE must be terminated to circuit ground, except during device programming or debugging.
3. Unused I/O pins are designated as outputs by ALS and are driven low.
4. All unassigned pins are available for use as I/Os.

Package Pin Assignments (continued)

T-46-19-11



Notes:

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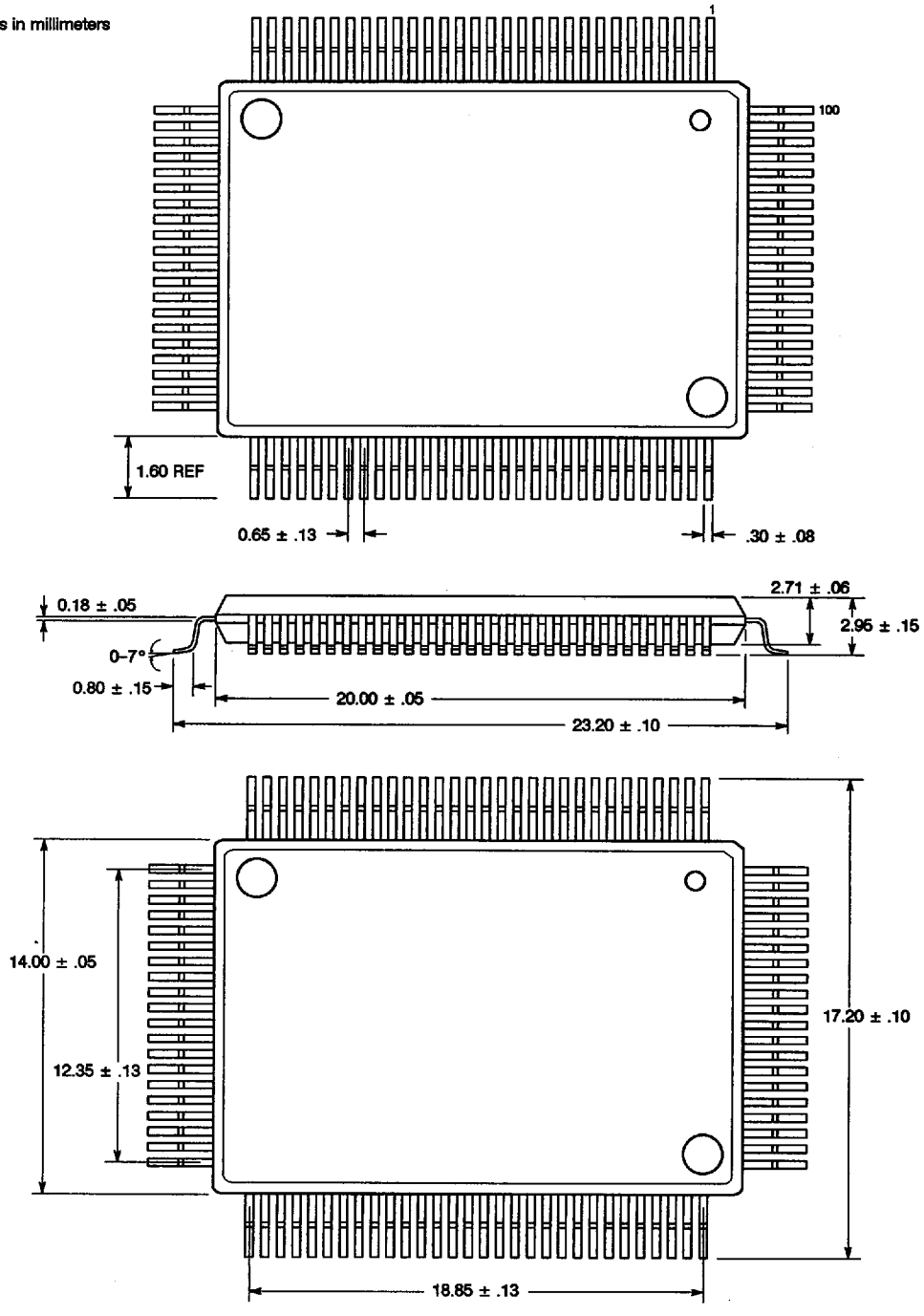
4. All unassigned pins are available for use as I/Os.

Package Mechanical Details (continued)

Plastic Quad Flatpack

T-46-19-11

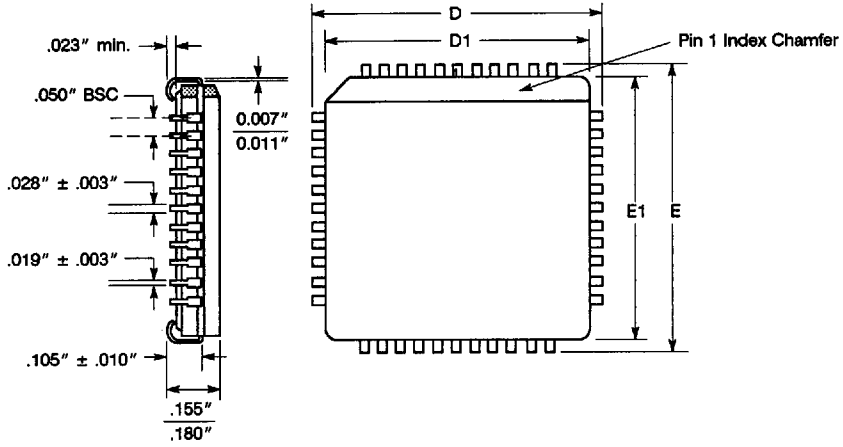
Dimensions in millimeters



Package Mechanical Details

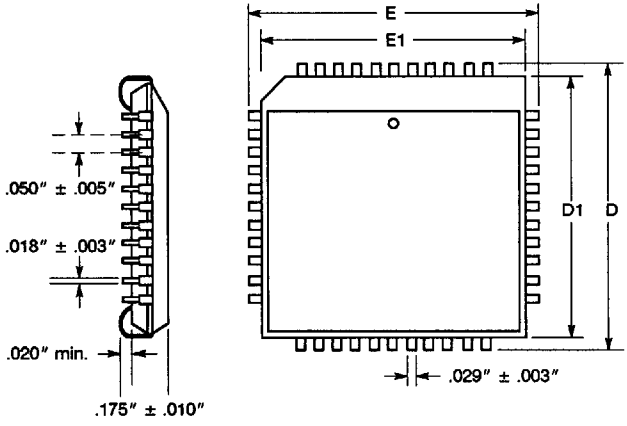
J-Leaded Cerquad Chip Carrier

T-46-19-11



Lead Count	D, E	D1, E1
44	.690" ± .005"	.650" ± .008"
68	.990" ± .005"	.950" ± .008"
84	1.190" ± .005"	1.150" ± .008"

Plastic J-Leaded Chip Carrier

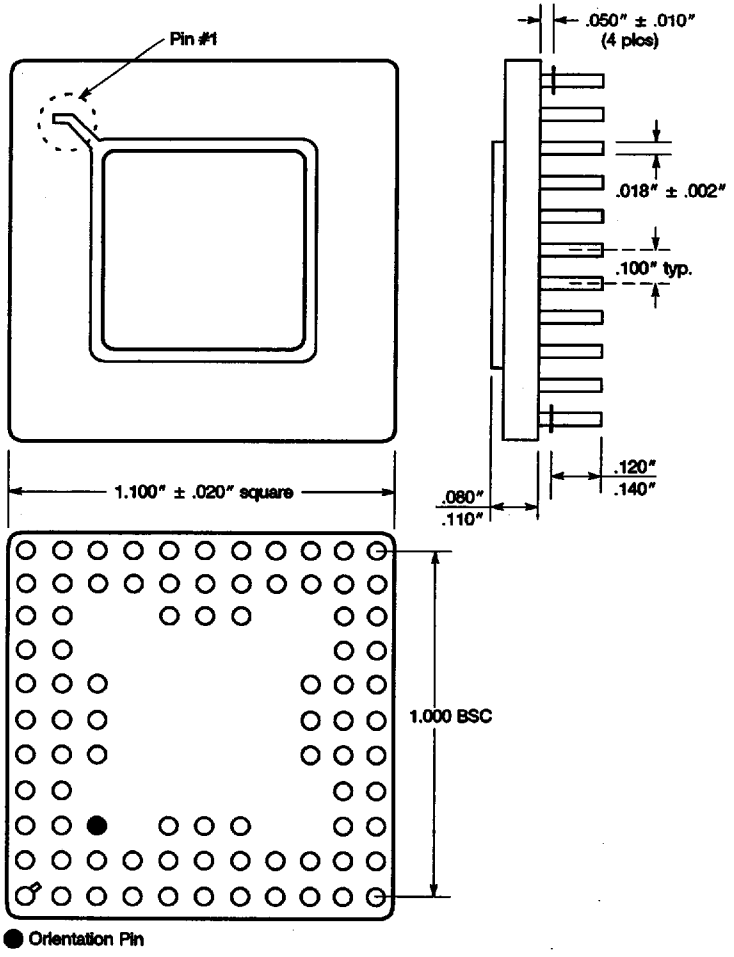


Lead Count	D, E	D1, E1
44	.690" ± .005"	.655" ± .005"
68	.990" ± .005"	.955" ± .005"
84	1.190" ± .005"	1.155" ± .005"

Package Mechanical Details (continued)

T-46-19-11

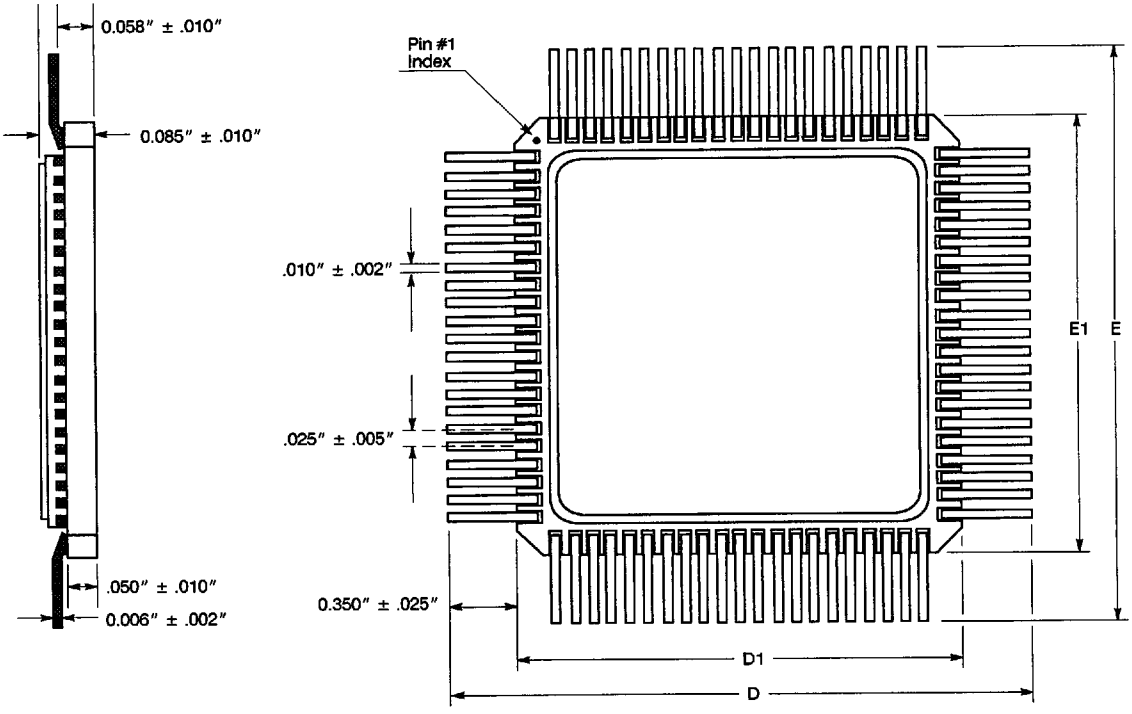
Ceramic Pin Grid Array



Package Mechanical Details (continued)

Ceramic Quad Flatpack

T-46-19-11



Lead Count	D, E	D1, E1
84	1.350" ± .030"	0.650" ± .010"