# Development Board EPC9205 Quick Start Guide

*eGaN® FET Power Module, Using 100 V EPC2045*

Revision 1.0

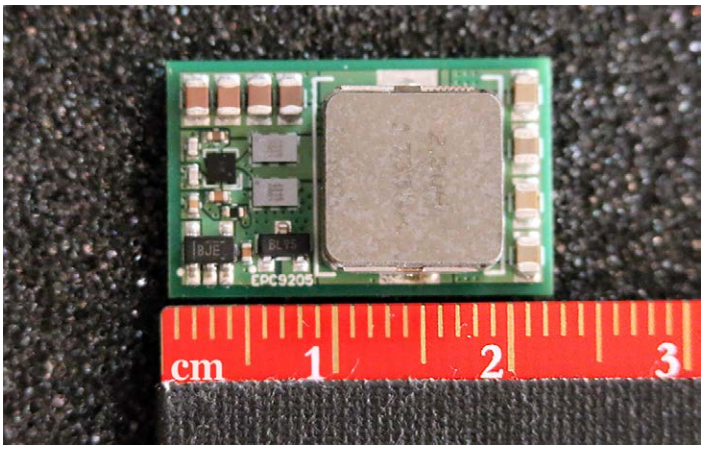
EFFICIENT POWER CONVERSION

## DESCRIPTION

The EPC9205 development board provides an eGaN FET based power module, featuring the EPC2045 eGaN FET (Enhancement-mode Gallium Nitride Field Effect Transistor). The purpose of this development board is to simplify the evaluation process of the EPC2045 eGaN FET by including all the critical components on a single board that can be easily connected into any existing system.

The EPC9205 development board is 13.5 mm x 22 mm x 5 mm and contains two EPC2045 eGaN FETs in a half-bridge configuration, i n combination with the UPI UP1966A gate driver. The board also contains all critical components and layout for optimal switching performance. A block diagram of the circuit is given in Figure 1.

For more information on the EPC2045, please refer to the datasheet available from EPC at www.epc-co.com. The datasheet should be read in conjunction with this quick start guide.




**EPC9205 Top View**

**Table 1: Performance Summary ($T_A$ = 25°C) EPC9205**

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Gate Drive Input Supply Range | | 4.5 | 5 | 5.5 | V |
| $V_{IN}$ | Bus Input Voltage Range (1) | | | 48 | 80 | V |
| $I_{OUT}$ | Switch Node Output Current (2) | | | 10 | | A |
| $f_{sw}$ | Target Switching Frequency | | | 700 | | kHz |
| $V_{PWM}$ | PWM Logic Input Voltage Threshold | Input 'High'<br>Input 'Low' | 2.3<br>0 | | 5<br>0.5 | V<br>V |
| | Minimum 'High' State Input Pulse Width | $V_{PWM}$ rise and fall time < 10 ns | 25 | | | ns |

*(1) Maximum switch node ringing must be kept under 100 V for EPC2045.*
*(2) Maximum current depends on die temperature – actual maximum current with be subject to switching frequency, bus voltage and thermal cooling.*

## QUICK START PROCEDURE

Development board EPC9205 is easy to set up to evaluate the performance of the EPC2045 eGaN FET. Refer to Figure 10 for pin descriptions, and follow the procedure below:

1. With power off, connect the input power supply bus to $+V_{IN}$ and ground / return to PGND.
2. With power off, connect $+V_{OUT}$ to your circuit as required.
3. With power off, connect the gate drive input to $+V_{CC}$ and ground return to AGND.
4. With power off, connect the input PWM control signals to HIN and LIN referenced to AGND. Note: This board does not have shoot-through protection and it is recommended to use a larger initial dead-time, or blanking period between the HIN and LIN signals to begin. Once converter operation is verified, the dead-time can be reduced to a value determined by the user. The EPC recommended dead-time for the typical operating conditions is 10 ns for each edge, shown in figure 2.
5. Turn on the gate drive supply – make sure the supply is between 4.5 V and 5.5 V range.
6. Turn on the controller / PWM input source for both high-side and low-side FETs.
7. Turn on the bus voltage to the required value (do not exceed the absolute maximum voltage).
8. Once operational, adjust the PWM control, bus voltage, and load within the operating range and observe the output switching behavior, efficiency and other parameters.
9. For shutdown, please follow steps in reverse.

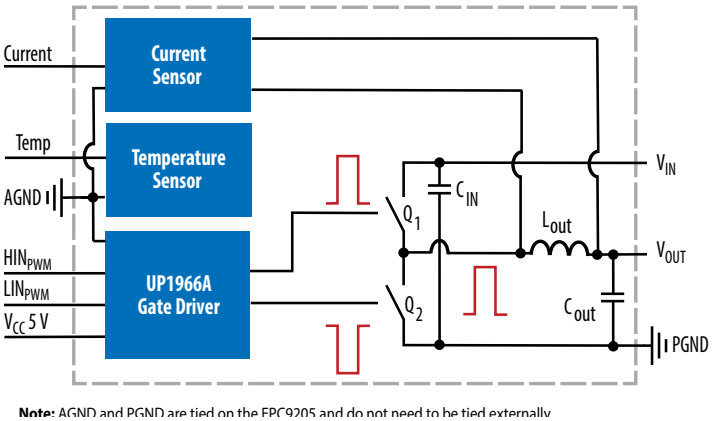



Figure 1. Block Diagram of EPC9205 Development Board.

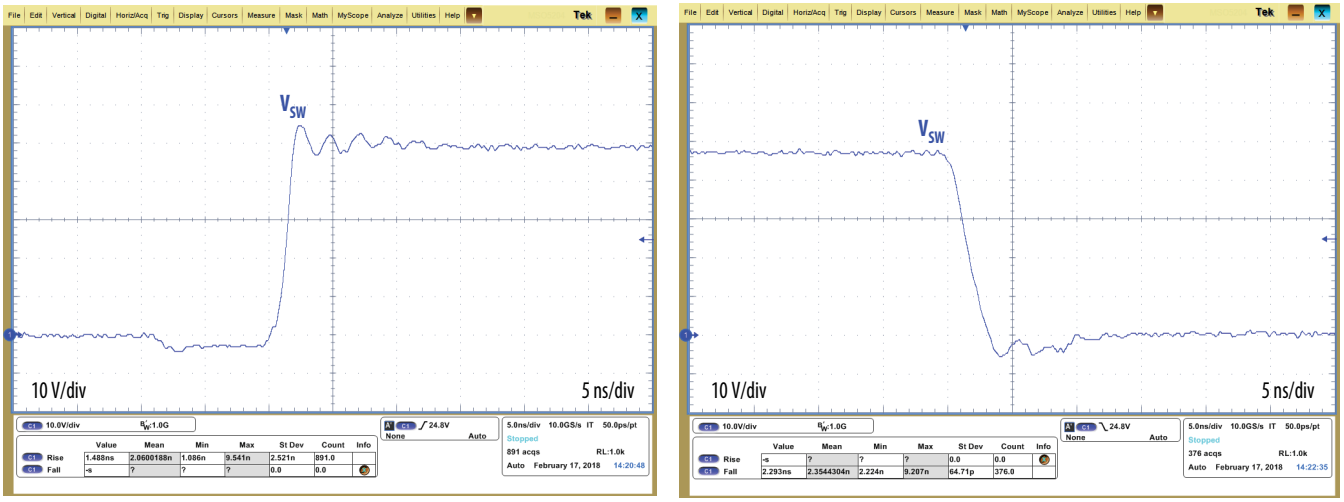
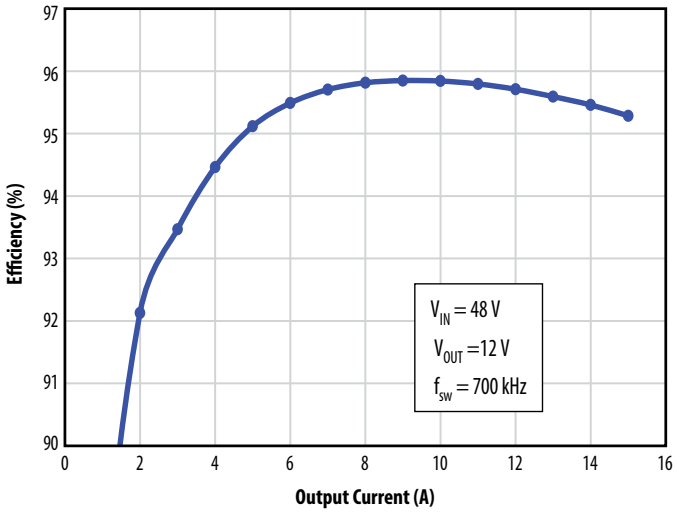



Figure 2: Typical Waveform for $V_{IN}$ = 48 V to 12 $V_{OUT}$, 10 A, 700 kHz Buck Converter




**Note:** Total system efficiency including power stage, inductor, driver, capacitors, and PCB losses.

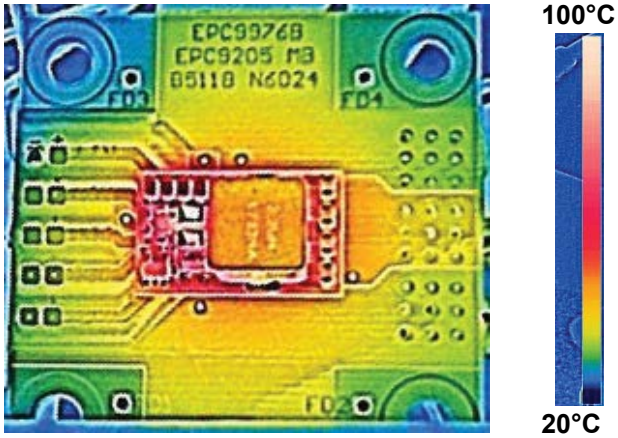
Figure 3: Typical System Efficiency for $V_{IN}$ = 48 V to 12 $V_{OUT}$ Buck Converter

## THERMAL CONSIDERATIONS

The EPC9205 development board showcases the EPC2045 eGaN FET. The EPC9205 is intended for bench evaluation. The addition of heat-sinking and forced air cooling can significantly increase the current rating of these devices, but care must be taken to not exceed the absolute maximum die temperature of 150° C. An example thermal image is shown in Figure 4 for typical operating conditions.

For more information regarding the thermal performance of EPC eGaN FETs, please consult:

D. Reusch and J. Glaser, *DC-DC Converter Handbook*, a supplement to GaN Transistors for Efficient Power Conversion, First Edition, Power Conversion Publications, 2015.




**Note:** Max eGaN FET case temperature = 100°C

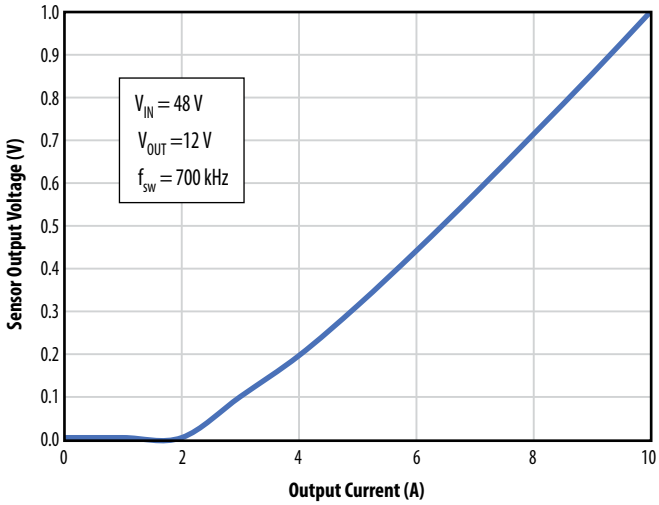
Figure 4: Thermal image for $V_{IN}$ = 48 V to 12 $V_{OUT}$, 10 A, 700 kHz, 400 LFM airflow.

## CURRENT & TEMPERATURE SENSING

The EPC9205 includes an optional output current sensing circuit using the TI INA196 current shunt monitor, which is disabled by default. To enable the sensor, optional components $R_s$ and $C_s$ can be populated with 1.6 kΩ and 150 nF respectively, as specified in the BOM below. Enabling this circuit contributes approximately 200 mW of additional power loss to the EPC9205. The output voltage characteristic of this sensing circuit on the EPC9205 is shown in Figure 5.

The EPC9205 also includes temperature sensing, using the Microchip TC1047A precision temperature-to-voltage converter. An example output voltage characteristic of this sensor on the EPC9205 is shown in Figure 6.

**Note:** The on-board temperature sensor reflects the temperature of the PCB. The relationship between sensor output voltage and eGaN FET temperature may vary with operating conditions and thermal design, and it should be calibrated for a given test setup. Figure 6 shows an example of this calibration curve in one test case.




**Note:** Current sense is optional on this development board and not enabled by default.

Figure 5: Current Sensor Output Curve for EPC9205 Development Board with $V_{IN}$ = 48 V to 12 $V_{OUT}$, 700 kHz

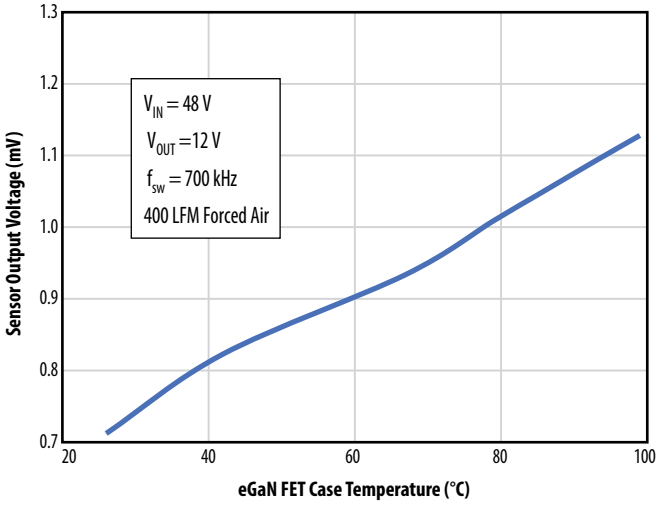



Figure 6: Example Temperature Sensor Output Curve for EPC9205 Development Board with $V_{IN}$ = 48 V to 12 $V_{OUT}$, 700 kHz, 400 LFM Forced Air Cooling

## DESIGN CONSIDERATIONS

To improve the electrical and thermal performance of the EPC9205 development board, some design considerations are recommended:

1. Large copper planes should be connected to the development board to improve thermal performance as shown in Figures 7 and 8. If filled vias are used in the board design, thermal vias should be placed under the device to better distribute heat through buried inner layers. For a design without filled vias, thermal vias should be located outside of the development board.
2. The gate drive ground return connection (AGND, pin 4 in mechanical drawings), is connected on the EPC9205 board should be isolated from the power ground connection (pins 7,8,9,11 in mechanical drawings).
3. If additional input filter capacitance is required, it can be placed outside the module. Due to the internal on-board input capacitance, minimizing the distance of the additional input capacitors to the development board, while preferred, is not a design requirement.

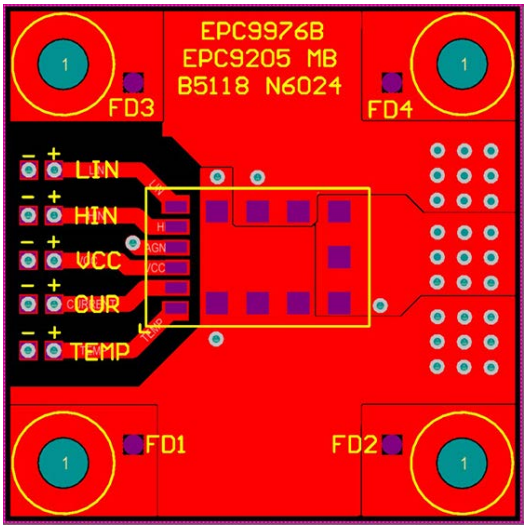



Figure 7: Top layer without filled thermal vias.

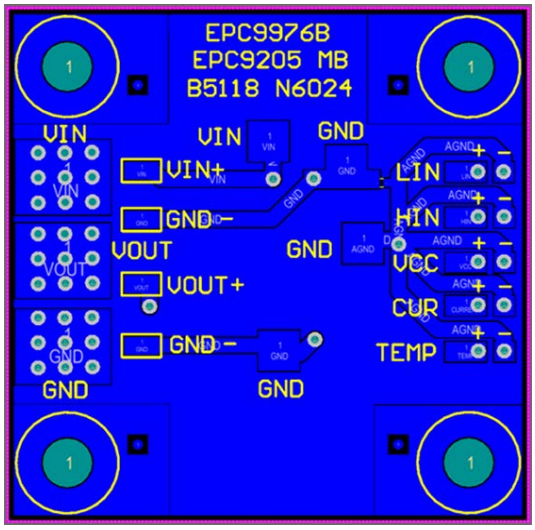
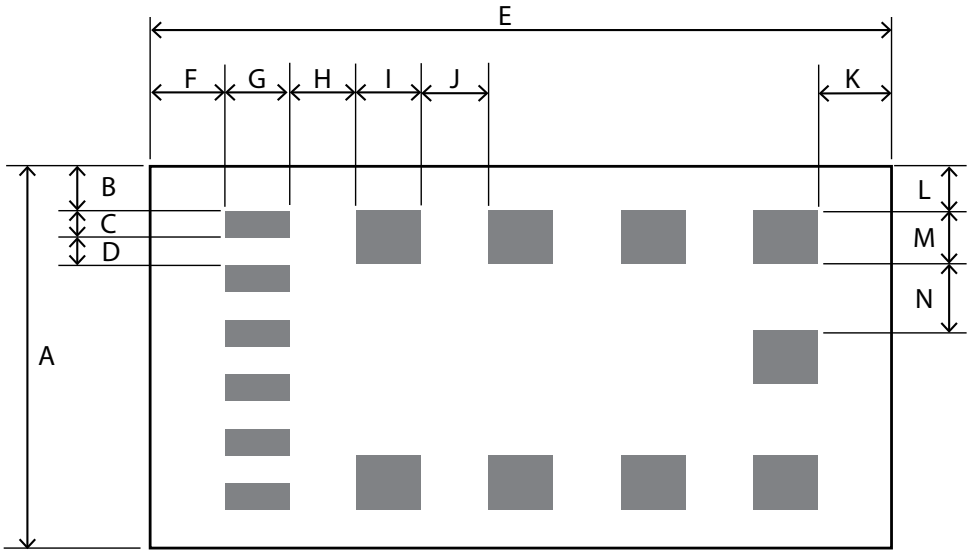


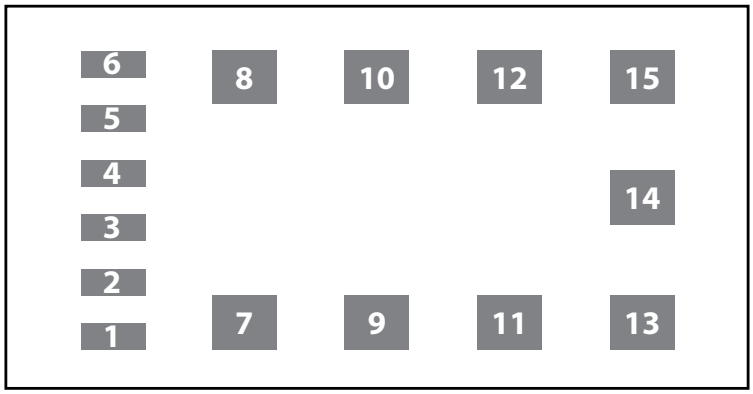

Figure 8: Bottom layer layout.

## MECHANICAL DATA




| Symbol | Dimension |
|---|---|
| A | 13.6 mm |
| B | 1.3 mm |
| C | 1 mm |
| D | 1 mm |
| E | 22 mm |
| F | 2 mm |
| G | 2 mm |
| H | 2 mm |
| I | 2 mm |
| J | 2 mm |
| K | 2 mm |
| L | 1.3 mm |
| M | 2 mm |
| N | 2.5 mm |

Figure 9: Footprint mechanical outline and pin numbering. (Top view)




| Pin | Type |
|---|---|
| 1 | Temp |
| 2 | Current |
| 3 | $V_{CC}$ |
| 4 | AGND |
| 5 | $HIN_{PWM}$ |
| 6 | $LIN_{PWM}$ |
| 7, 8, 9, 11 | PGND |
| 10, 12 | $V_{IN}$ |
| 13, 14, 15 | $V_{OUT}$ |

Figure 10: Pin Descriptions. (Top view)

**Table 2: Bill of Materials**

| Item | Qty | Reference | Part Description | Manufacturer | Part # |
|---|---|---|---|---|---|
| 1 | 4 | CIN1, CIN2, CIN3, CIN4 | Cap, ceramic, 1µF, 100 V, X7S, 0805 | TDK | C2012X7S2A105M125AB |
| 2 | 2 | Q1, Q2 | eGaN FET, 100 V | EPC | EPC2045 |
| 3 | 1 | CB | Cap, ceramic, 0.1 µF, 25 V, X5R, 0402 | TDK | C1005X5R1E104K050BC |
| 4 | 2 | CDEC, CDEC2 | Cap, ceramic, 1 µF, 25 V, X5R, 0402 | TDK | C1005X5R1E105K050BC |
| 5 | 2 | CDEC3, CDEC4 | Cap, ceramic, 22 pF, 50 V, C0G, 0402 | Kemet | CBR04C220F5GAC |
| 6 | 1 | U1 | Gate Drive IC, dual | UPI | uP1966A |
| 7 | 4 | COUT1, COUT2, COUT3, COUT4 | Cap, ceramic, 22 µF, 25 V, X5R, 0805 | Murata | GRT21BR61E226ME13L |
| 8 | 1 | L1 | Inductor, 2.2 µH, 20%, 12 A | Vishay | IHLP4040DZER2R2M01 |
| 9 | 1 | U3 | Temperature sensor IC, analog | Microchip | TC1047AVNBTR |
| 10 | 1 | U2 | Current sense amplifier IC | TI | INA196AIDBVR |

**Table 3: Optional Components**

| Item | Qty | Reference | Part Description | Footprint |
|---|---|---|---|---|
| 1 | 1 | CS | Capacitor, ceramic, 15 nF, 16 V | 0402 |
| 2 | 1 | RS | Res, 1.62 k, 1/16 W | 0402 |

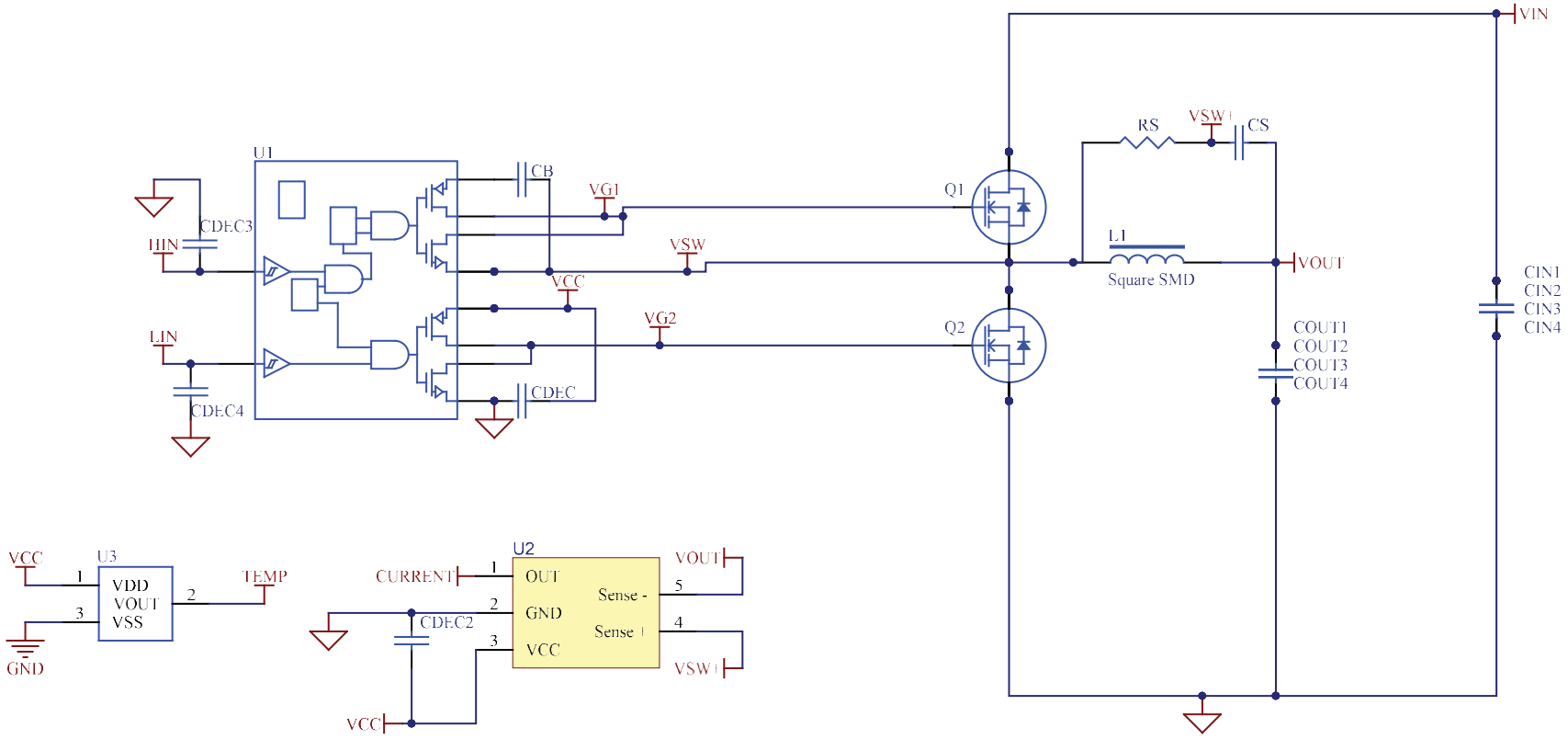



Figure 11: EPC9205 schematic

## For More Information:

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The EPC9205 board is intended for product evaluation purposes only and is not intended for commercial use. Replace components on the Evaluation Board only with those parts shown on the parts list (or Bill of Materials) in the Quick Start Guide. Contact an authorized EPC representative with any questions.

This board is intended to be used by certified professionals, in a lab environment, following proper safety procedures. Use at your own risk.

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