## Features

- Ultra-low power Real-Time Clock (RTC) with power-fail detect and battery management
- Low power timer and power manager extend run time in battery-powered systems
- Controls 4.1V rechargeable micro-batteries and 3.2V rechargeable coin cells and supercaps; no off-chip components required for battery charger
- Buck charge pump extends backup battery life:
  - 15nA RTC using internal RC oscillator
  - 50nA RTC using crystal oscillator
- Counters for hundredths, seconds, minutes, hours, date, month, year, century, and weekdays based on a 32.768KHz crystal oscillator or internal RC oscillator
- Automatic leap year calculation
- Alarm capability on all counters
- Two configurable multi-use outputs for interrupts, output clock, and managing sleep mode of external devices
- 64 bytes of RAM
- Internal temperature measurement with 10-bit ADC enables oscillator temperature compensation and temperature read-out
- Advanced crystal calibration to ± 1 ppm
- Ultra-low Iq VIN POR circuit (< 25nA)
- Fixed indicators for PGOOD, charging current on, and charging disabled
- Temperature range -40°C to +85°C
- Serial communication: $I^2C$-bus and SPI options
- Lead-free and halogen-free

## Applications

- **Power bridging** to provide uninterruptible RTC function during exchange of main batteries.
- **Consumer appliances** - CBC921 controls switchover from main supply to backup battery.
- **Ultra-low power timer** draws only 15nA
- **Wireless sensors and RFID tags** and other powered, low duty cycle applications.
- **Business and industrial systems** such as: network routers, point-of-sale terminals, single-board computers, test equipment, multi-function printers, industrial controllers, and utility meters.
  - Reliable system timekeeping
  - Battery-powered devices
  - Internet of Things, portable devices
  - Daily alarms


***3mm x 3mm x 0.55mm 16-pin MLPQ Package***

## General Description

The CBC921xx combines a real-time clock (RTC) with a backup battery charger and other power management features. In the event of an outage of the primary power source, automatic switchover to the backup battery enables extended timekeeping and optionally provides power to external devices to maintain their operation during the power outage.

In normal operation the RTC function is supported by a primary power source, which can be a battery cell, multiple alkaline batteries, or a regulated power supply ranging from 2.85V to 5.5V. The backup battery is charged with a temperature-compensated voltage derived from the primary voltage source. The backup battery charging is refreshed with a configurable schedule and temperature-dependent duty cycle, both of which are designed to increase service life of the backup battery while minimizing power consumption from the main power source.

The circuit can be used in applications to provide an uninterrupted continuous time clock, calendar function, and time-based interrupts or alarms for wake up from sleep to active mode operation with adjustable intervals to save power in the overall system.

The power management has a low quiescent current and high efficiency for backup battery charging. The RTC circuit has very low quiescent current to extend the RTC run time. The RTC has 2ppm accuracy for clock, calendar, alarm, clock outputs, and interrupt functions. An open drain internal power switch is controlled by interrupts and a sleep manager to facilitate power saving by disconnecting main power from external devices according to user-defined schedules.

# Contents

## Figures



## Tables

## Typical Application Circuit

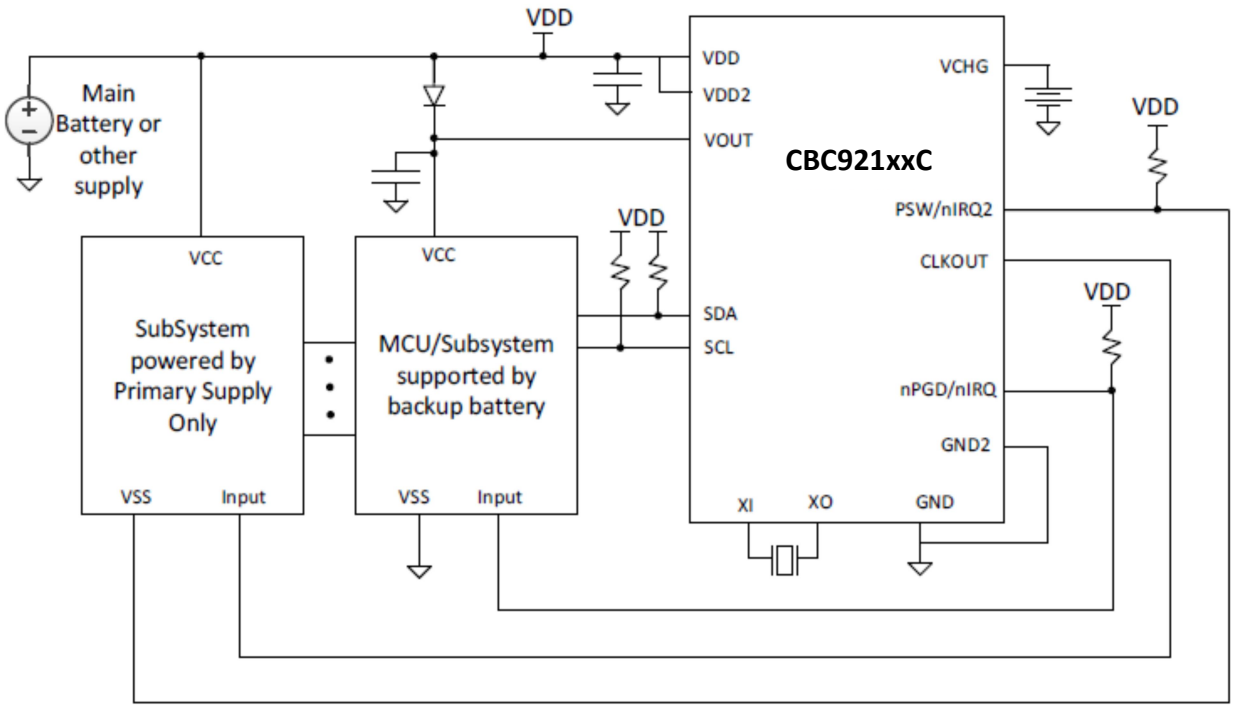
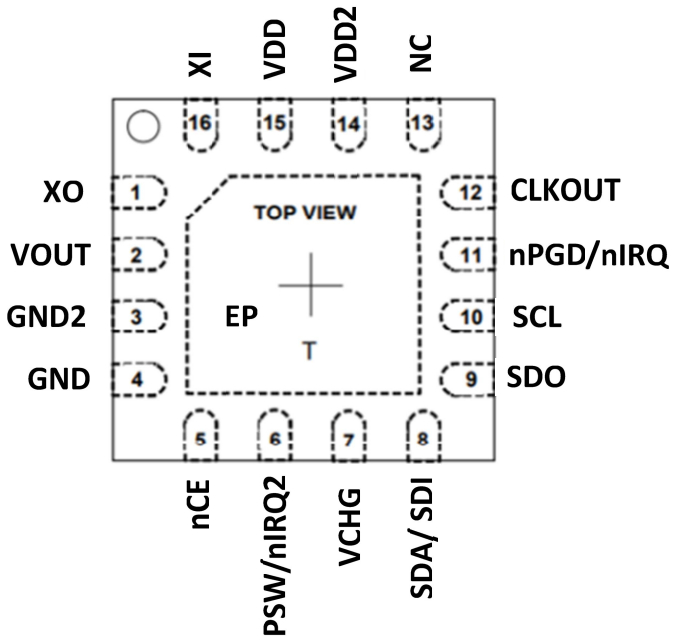



**Figure 1: Typical application circuit for CBC921xxC**

## Pin Configuration (MLPQ-UT16)




## Part Numbers

| Part Number | RTC | PM | I/F | Charge Voltage |
|---|---|---|---|---|
| CBC92100C | Y | | I²C | |
| CBC92100P | Y | | SPI | |
| CBC92032C | | Y | I²C | 3.2V |
| CBC92041C | | Y | I²C | 4.1V |
| CBC92032P | | Y | SPI | 3.2V |
| CBC92041P | | Y | SPI | 4.1V |
| CBC92132C | Y | Y | I²C | 3.2V |
| CBC92141C | Y | Y | I²C | 4.1V |
| CBC92132P | Y | Y | SPI | 3.2V |
| CBC92141P | Y | Y | SPI | 4.1V |

| CBC92XYYZ Part Numbering | |
|---|---|
| X | 1=RTC included, 0=no RTC |
| YY | Maximum battery charging voltage (x 10), 00=no battery management included |
| Z | C=I²C, P=SPI |

# Absolute Maximum Ratings

| Parameter | Symbol | Value | Units |
|---|---|---|---|
| External Supply Input (VDD) | $V_{DD}$ to $V_{GND}$ | -0.3 to +6.0 | V |
| Battery Connection Pin (VCHG) | $V_{CHG}$ to $V_{GND}$ | -0.3 to +4.15 | V |
| Supply Output Voltage Pin (VOUT) | $V_{OUT}$ to $V_{GND}$ | -0.3 to +6.0 | V |
| XI, XO pins in VDD Mode | $V_{XT\_VDD}$ to $V_{GND}$ | -0.3 to VDD +0.3 | V |
| XI, XO pins in Backup Mode | $V_{XT\_BAT}$ to $V_{GND}$ | -0.3 to VCHG +0.3 | V |
| VDD2 pin to VDD pin | $V_{DD2}$ to $V_{DD}$ | -0.3 to +0.3 | V |
| GND2 pin to GND pin | $V_{GND2}$ to $V_{GND}$ | -0.3 to +0.3 | V |
| SCL, SDA/SDI, PSW/nIRQ2, nPGD/IRQ, nCE pins | $V_{IO1}$ to $V_{GND}$ | -0.3 to +6.0 | V |
| CLKOUT and SDO pins, in Backup and VDD Modes | $V_{IO2}$ to $V_{GND}$ | -0.3 to VDD +0.3 | V |
| PSW/nIRQ2 pin current | $I_{PSW}$ | 200 | mA |
| ESD Protection Level (HBM), VCHG pin (1) | $V_{CHG\_ESD}$ to $V_{GND}$ | TBD | kV |
| ESD Protection Level (HBM), all other pins (1) | $V_{IO\_ESD}$ to $V_{GND}$ | 2 | kV |
| Operating Temperature | $T_J$ | -40 to +85 | °C |
| Storage Temperature | $T_{STG}$ | -65 to +150 | °C |

Notes:
Exceeding the above specifications may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

Notes:
(1): Tested according to JEDEC standard JESD22-A114-B. No ESD protection is guaranteed on the VCHG pin.

# Thermal Characteristics

| Parameter | Symbol | Value | Units |
|---|---|---|---|
| Thermal Impedance(2) | $R_{\theta JA}$ | 50 | °C/W |

Notes:
(2): Calculated from package in still air, mounted to 3 x 4.5 (in), 4 layer FR4 PCB per JESD51 standards.

# Electrical Characteristics

Unless otherwise specified: $T_J < 85°C$, $-40°C < T_A < +85°C$, VDD = 3.6 V, 1uF VDD to GND. Typical values are for $T_A = +25°C$

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| **Supply Range** | | | | | | |
| VDD Supply Voltage Range | Vdd | | $V_{POR\_rising\_MAX}$ | | 5.5 | V |
| VDD Power-on Reset Rising Threshold | $V_{POR\_rising}$ | Backup to VDD mode entry threshold. | | 2.7 | 2.85 | V |
| VDD Power-on Reset Falling Threshold | $V_{POR\_falling}$ | Battery backup entry threshold. | 2.5 | | | V |
| VDD Power-on Reset Threshold Hysteresis | $V_{POR\_hysteresis}$ | $V_{POR\_rising}$ - $V_{POR\_falling}$. | 90 | 125 | 170 | mV |
| VDD POR rising indicator delay, from cutoff mode | $Td_{PGD\_cutoff}$ | Measured from VDD crossing $V_{POR\_rising}$ to the falling edge of the nPGD/nIRQ pin, VCHG=2.5V. | | 300 | | ms |
| VDD POR rising indicator delay, from backup mode | $Td_{PGD\_backup}$ | Measured from VDD crossing $V_{POR\_rising}$ to the falling edge of the nPGD/nIRQ pin, VCHG=4V. | | 80 | | ms |
| Battery Charging Delay Time | $Td_{CHG\_rising}$ | Measured from falling edge of the nPGD/nIRQ pin to rising edge of CHG pin. | | 40 | | ms |
| VOUT Cut-in Time Delay | $Td_{VOUT\_rising}$ | Measured from VDD crossing $V_{POR\_falling}$ threshold to the VOUT switch turn-on. | | 1 | | ms |
| **Supply Currents** | | | | | | |
| VCHG Supply Current, RC Mode, with Cutoff Monitor Inactive | $I_{CHG\_RC4}$ | Includes RTC operating in RC mode. 4.1V version. VCHG =4.1V. VDD=0 V. | | 20 | | nA |
| VCHG Supply Current, RC Mode, with Cutoff Monitor Inactive | $I_{CHG\_RC3}$ | Includes RTC operating in RC mode. 3.2V version. VCHG =3.2V. VDD=0V. | | 60 | | nA |

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| VCHG Supply Current, XT Mode, with Cutoff Monitor Inactive | $I_{CHG\_Xtal4}$ | Includes RTC operating in XTAL mode. 4.1V version. VCHG =4.1V. VDD=0V. | | 50 | | nA |
| VCHG Supply Current, XT Mode, with Cutoff Monitor Inactive | $I_{CHG\_Xtal3}$ | Includes RTC operating in XTAL mode. 3.2V version. VCHG =3.2V. VDD=0V. | | 150 | | nA |
| VCHG Supply Current, XT Mode, with Cutoff Monitor Active | $I_{CHG\_XtalMon}$ | Includes RTC operating in XTAL mode. 4.1V version only. VCHG =4.1V, VDD=0V. | | 350 | | nA |
| VDD Supply Current with Battery Charging | IddCharge | After POR rising. Excludes battery charging current, but including RTC in Xtal mode. nCE pin held at VDD. SDA/SDI and SCL pins held at VDD or GND. $I^2C$ bus inactive, other I/O's. not | | 4000 | | nA |
| VDD Supply Current with Battery NOT Charging | | After POR rising RTC operating in XTAL mode. I2C bus inactive. Other I/O's static. nCE pin held at VDD. SDA/SDI are high or low. No load on CLKOUT/CHGDIS. | | | | |
| VDD Supply Current in Backup Mode | IddPrePor | VDD=2.5V. | | 25 | | nA |
| CHG leakage Current, Cutoff Mode | $I_{CHG\_Cutoff}$ | VHG=2.5V. VDD=0V. 4.1V version only. | | 70 | | pA |
| **Battery Charger** | | | | | | |
| Battery Charger Output Current | $I_{CHG\_charge}$ | VCHG=3V. | | 50 | | uA |
| Battery Charger Output Voltage | $VCHG_4$ | 25°C, VDD> $V_{POR\_rising\_MAX}$, 4.1V version. | 4.025 | 4.075 | 4.1 | V |
| Battery Charger Output Voltage | $VCHG_3$ | 25°C, VDD > $V_{POR\_rising\_MAX}$, 3.2V version. | 3 | 3.1 | 3.2 | V |
| Battery Charger Output Voltage TC | $VCHG_{Tc4}$ | 25°C to 85°C, 4.1V version. | | -2.2 | | mV/degC |
| Battery Charger Output Voltage TC | $VCHG_{Tc3}$ | 25°C to 85°C, 3.2V version. | | -1.67 | | mV/degC |
| Battery Cutoff Threshold | $VCHG_{Cutoff}$ | 4.1V version only. | 2.7 | 3 | 3.3 | V |
| **Oscillator** | | | | | | |
| RC Oscillator Frequency | $F_{RC}$ | Ta=25 °C. | | 256 | | Hz |

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| RC Oscillator Frequency Accuracy | FRC_TOL | Without calibration; supply between 2.9V and 5.5V | -4 | | +4 | % |
| Crystal oscillation frequency | $F_{XO}$ | | | 32768 | | Hz |
| Crystal Internal Load Capacitance | $CL_{INT}$ | | | 2.5 | | pF |
| Crystal Negative Resistance | $R_{NEG}$ | | | 520 | | kΩ |
| **Interface Logic** | | | | | | |
| Logic Input High Threshold | $V_{IH}$ | VDD=5.5V | 1.6 | | | V |
| Logic Input Low Threshold | $V_{IL}$ | VDD=2.9V | | | 0.4 | V |
| Logic Output High Level | $V_{OH}$ | CMOS outputs | | | | V |
| Logic Output Low Level | $V_{OL}$ | IL<3mA | | | 0.4 | V |
| Logic Input Leakage | $I_{dig\_leak}$ | | | < 1 | | nA |
| **Switch On-Resistance** | | | | | | |
| PSW/nIRQ2/nCHGON Pull Down Resistance | $R_{PSW}$ | I_load=100mA | | 4 | | Ω |
| VOUT Switch Resistance | $R_{VOUT}$ | $V_{CHG}$=4.1V, I_load=1µA | | 1 | | MΩ |
| **Serial Interface** | | | | | | |
| $I^2C$ Clock Frequency | FI2C | | | | 400 | kHz |

# Pin Descriptions

| Pin # | Pin Name | Pin Type | Pin Function (for PM-RTC versions with I²C or SPI) |
|---|---|---|---|
| 1 | XO | Analog output (high-Z) | Crystal oscillator connection high-impedance node. Minimize trace length between the crystal and the I.C. |
| 2 | VOUT | Supply Output | Output voltage providing bias to external circuits in backup mode only. Enabled by VOUTEN register bit. A high-resistance switch and series diode feeding this pin limit the output current and protect the battery. |
| 3 | GND2 | Ground | This pin must be connected to ground (GND). |
| 4 | GND | Ground | Ground |
| 5 | nCE | Digital Input (CMOS) | Chip Enable for SPI. Connect this pin to ground when using the I²C version. |
| 6 | PSW/nIRQ2 | Output - Open Drain | Configurable open-drain output. This pin has a low-resistance switch to ground which can be connected to the ground return of external devices to switch power to those devices. If no interrupt is enabled, PSWEN_WAKE=1, and no other function is configured by the Control Register 2, this pin has the default function of indicating with an active low output if the battery is currently being charged. |
| 7 | VCHG | Supply In/Out | Regulated voltage source output for backup battery charging. Power supply input in backup mode. Connect a battery or other energy storage device between this pin and GND. |
| 8 | SDA/ SDI | Digital I/O - Open Drain | Serial data input/output for I²C version. Serial data input for SPI version. A pull-up resistor is needed on this bus. A value between 5 KΩ and 100 KΩ is recommended depending on the clock frequency of the serial communications. |
| 9 | SDO | Digital Output (CMOS) | Serial data output for SPI version. Leave this pin open when using I²C version. |
| 10 | SCL | Digital Input (CMOS) | I²C clock/SPI clock |
| 11 | nPGD/nIRQ | Output - Open Drain | Configurable PGOOD indicator and interrupt1 output. Initially functions as a power good signal, going to an active-low state when the SC63xxx I/O's are ready. At this time, the pin function may be reconfigured by writing to the OUT1S bit through the serial port. Otherwise, this pin will follow the PGOOD register bit, staying active-low until VDD falls below the POR falling threshold. A pull-up resistor to VDD is required to use this pin. Use a maximum value of 200 MΩ, but a lower value may be needed for higher frequency output selections. |
| 12 | CLK OUT | Digital Output - CMOS | Programmable CMOS clock output. Until configured by the clock output control register, this pin has the default function of indicating (with output high) if charging is disabled by either the CHGOFF or CHGRST register bits. |

| Pin # | Pin Name | Pin Type | Pin Function (for PM-RTC versions with I2C or SPI) |
|---|---|---|---|
| 13 | NC | Open | Unused pin, not connected to the I.C. |
| 14 | VDD2 | Supply | This pin must be connected to the VDD pin. |
| 15 | VDD | Supply | Main power source input. Can be connected to the main battery or another voltage source. Place decoupling capacitor of at least 0.1uF between VDD and GND close to the I.C. |
| 16 | XI | Analog input | Crystal oscillator input; high-impedance node. Minimize trace length between the crystal and the I.C. |
| 17 | EP | Exposed Pad | Connect the exposed pad to GND. |

# Block Diagram

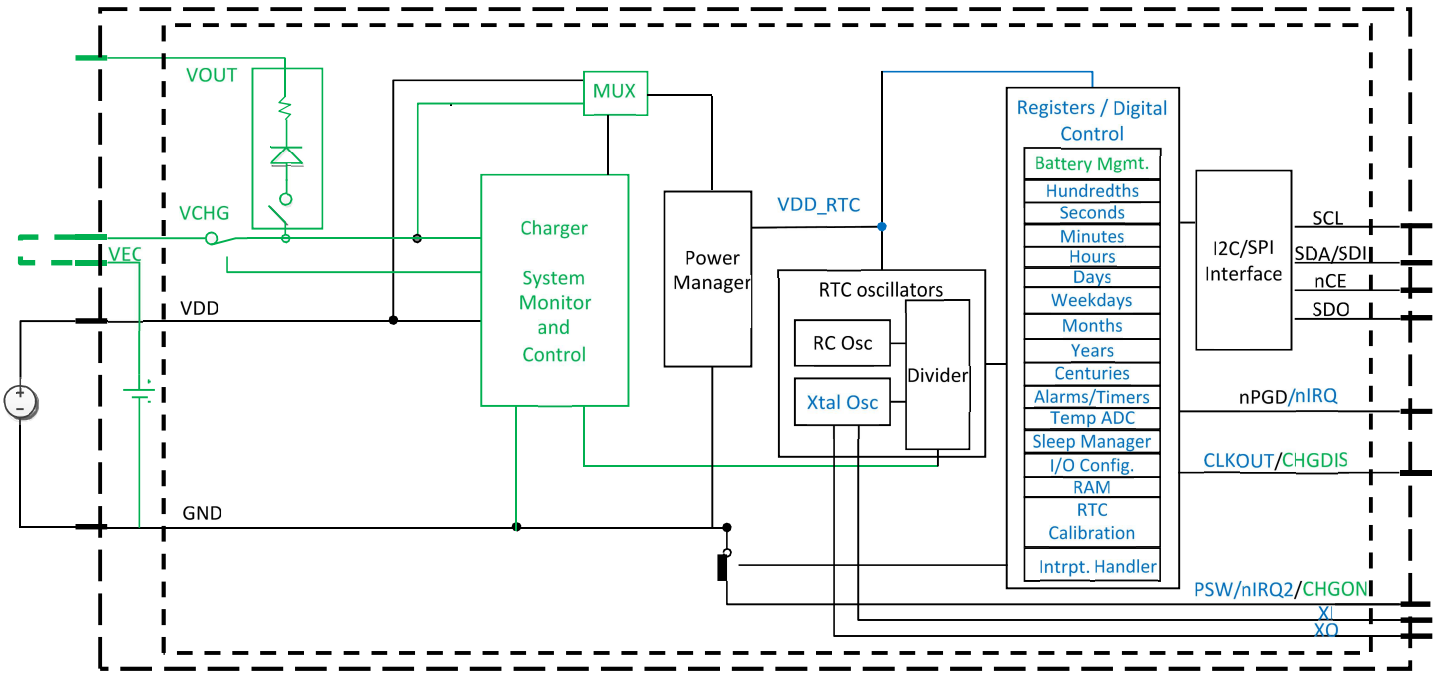



**Figure 2: PMRTC block diagram for bare-die version packaged with a battery**

# Functional Description

## Operating Modes and Transitions

The two operating modes of the CBC92141 are normal operation and backup mode. When the VDD pin is below the POR threshold, the CBC92141 is in backup mode. In backup mode, the CBC92141 operates in an ultra-lower power mode from a power source, typically a battery, connected to the VCHG pin to keep the real time clock running and, if requested and configured accordingly, to supply power to an external load at the VOUT pin. The I/O pins are not available in backup mode, so there are no interrupts or serial communications in this mode The 4.1V version (CBC92141) will shut down to protect the backup battery from over-discharge if the battery voltage falls below the VBatt_off threshold.

The CBC92141 will be in a non-operational cutoff state initially and whenever the battery voltage falls below the cutoff threshold while VDD is also below the POR threshold. VDD must rise above the POR threshold in order to exit the cutoff state. Figure 9 below illustrates the operating mode transitions and power states.

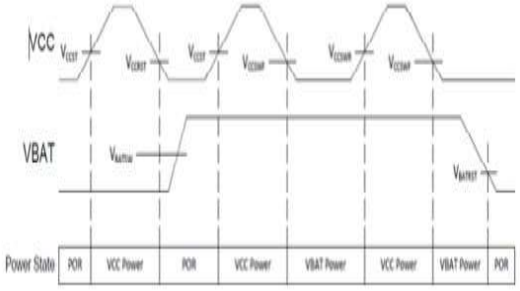



**Figure 3 Power States and Operating Mode Transitions**

## VDD Mode Entry Sequence

When the external VDD supply rises above the POR threshold, the CBC92141 enters normal operation after a delay $Td_{PGD}$, as shown below in Figure **10**. The duration of the $Td_{PGD}$ delay depends on whether the CBC92141 is coming out of backup mode or cutoff mode. After the applicable $Td_{PGD}$ delay, the nPGD/nIRQ pin will go to an active-low state, indicating that the CBC92141 has disconnected from the backup battery and that the I/O's are ready for communication and signaling. At this time, the external software should use the serial port to rewrite any application-specific values to registers that are not powered in backup mode. In the case of first-time power – up or coming out of cutoff, all application specific register values should be written at this time. After a delay of approximately 40ms the battery charging controller will begin operation. In normal operation the CBC921 will initially and periodically refresh the charge state of the backup battery with a charging voltage and temperature dependent duty cycle based on die temperature. If the OUT1S register bit is not changed the nPGD/nIRQ pin will continue to follow the PGOOD register bit staying active low until VDD falls below the POR falling threshold.

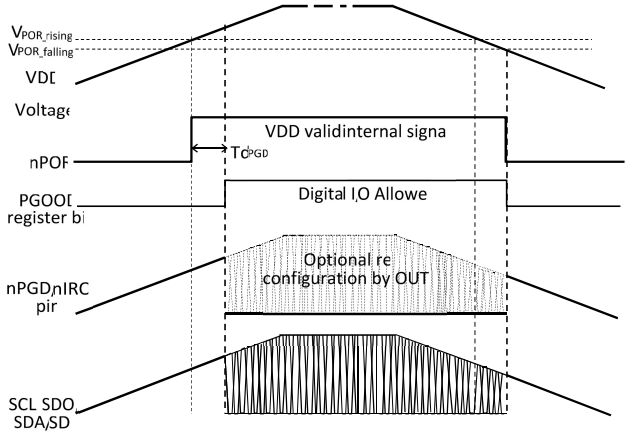



**Figure 4: VDD Mode Start Up and Shutdown Sequence**

## Registers and RTC Management

The RAM and the following registers are powered in backup mode:

- Access Control 0x10
- Charge Control 0x1B
- Battery Management 0x24

The following are both available and backed up only in the feature PMRTC version:

- Time and Alarm 0x00-0x0E
- Flags 0x0F
- Calibration 0x14-16
- Timer Control and Countdown Timer 0x18-19
- OSC and RTC Control 0x1C
- RTC data transfer registers 0x22 and 0x23

If the CBC92141 goes into backup mode while the RTC is stopped (e.g., due to resetting the time), it will be automatically restarted so that the system might determine the duration of the power outage and keep general track of time during the outage even if an adjustment was in process.

voltage and duty cycle that depends on the temperature measured in the CBC92141. If the OUT1S register bit is not changed, the nPGD/nIRQ pin will continue to follow the PGOOD register bit, staying active-low until VDD falls below the POR falling threshold.

Countdown, alarm and calibration timers will continue to run in backup mode, except the countdown timer will not repeat once it sets the CDT flag.

Registers not listed above, including any associated states such as SLEEP, will be reset to their default values, upon entering normal operation (VDD POR), except that the status register will be updated to reflect any pending interrupts resulting from alarm or countdown timer operations that continued through the backup mode. Also, any flags that were not yet cleared when VDD was lost will generate an interrupt upon return of VDD.

## Oscillator Selection and Verification

The CBC92141 generates an internal 256 Hz clock from one of two ultra-low power oscillators depending on the on the Operating state and the value of the OSEL bit in the Oscillator Control register. An OSEL bit value of 0 selects the internal 256 Hz oscillator, and a value of 1 selects the 32.786 kHz crystal (XT) oscillator. Upon initial power-up, the RC oscillator is used for timekeeping and internal logic The OSEL bit can be toggled by the serial communications port to switch between the RC and XT oscillators. The system might do this to reduce power consumption, which is lower using the RC oscillator, or if the system controller detects an XT frequency error well beyond the calibration capabilities of the system. Using the AOS register bit, the CBC92141 can be configured to automatically switch to the RC oscillator upon entering backup mode.

Switching between the XT and RC Oscillators is guaranteed to produce less than 10 milliseconds of error in the Calendar Counters., but this error could accumulate over time if there is frequent switching between the oscillators, as might be done to periodically check the functionality of the XT oscillator.

## I²C Interface

The CBC92141C has a slave I²C interface that supports standard and fast mode data rates and combined format operations and is compliant with the I²C standard version 6.0 April 2014.

## Limitations to the I²C Specifications

The CBC92141 only recognizes seven bit addressing. This means that ten bit addressing and CBUS communication are not compatible. The device can operate in either standard mode (100kbit/s) or fast mode (400kbit/s).

I²C is a two-wire serial interface where the two lines are serial clock (SCL) and serial data (SDA). SDA must be connected to a positive supply through an external pull-up resistor. The devices communicating on this bus can drive the SDA line low or release it to high impedance. An external device that initiates the I²C transaction becomes the master of the bus. Communication is initiated by the master sending a Start condition, a high-to-low transition on SDA, while the SCL line is high. After the Start condition, the device address byte is sent, most significant bit (MSB) first, including the data communications. The eighth bit is the data direction bit.

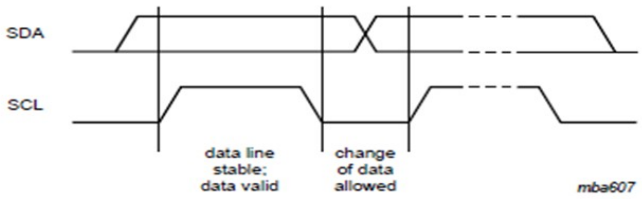



**Figure 5: Bit Transfer on the I2C Bus**

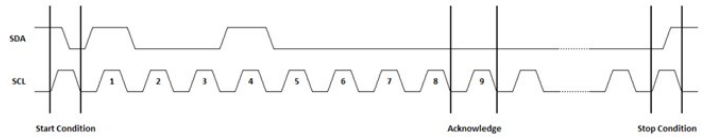



**Figure 6: I2C Start Stop Protocol**

## Slave I²C Address Assignment

The CBC92141 has the slave address byte 1010101x for I²C communications. The eight bit is the direction bit.

## Supported Formats

The supported formats are described in the following subsections and illustrated in the following subsections.

## (1) Direct Format — Write

The simplest format for an I²C write is direct format. After the start condition [S], the slave address is sent, followed by an eighth bit indicating a write. The CBC92141C then acknowledges that it is being addressed, and the master responds with an 8 bit data byte consisting of the register address. The slave acknowledges and the master sends the a 8-bit data byte to be written. Once again, the slave acknowledges and the master either terminates the transfer with the stop condition [P], as shown in , or sends additional 8 bit data bytes (each to be acknowledged by the slave) before terminating. Upon writing data to a register, the CBC92141C automatically increments the register address pointer for subsequent data received in the write operation.

## (2) Combined Format — Read

After the start condition [S], the slave address is sent, followed by an eighth bit indicating a write. The CBC92141C then acknowledges that it is being addressed, and the master responds with an 8-bit data byte consisting of the target register address. The slave acknowledges and the master sends the repeated start condition [SR]. Once again, the slave address is sent, followed by an eighth bit indicating a read. The slave responds with an acknowledge and the 8 bit data from the target register. If the master then sends an ACK, the slave will auto-increment the register address and send the 8-bit data from the new address. The ACK and auto-increment read may continue until the master terminates the read operation by sending a non-acknowledge (NACK) and terminating the transfer with the stop condition [P]. Figure 14 shows the Combined Format Read operation for the case in which a single byte is read.

## (3) Stop-Separated Reads

Stop-separated reads can also be used. This format allows a master to set up the register address pointer for a read and return to that slave at a later time to read the data. In this format the slave address followed by a write command are sent after a start [S] condition. The CBC92141C then acknowledges it is being addressed, and the master responds with the 8-bit register address. The master sends a stop or restart condition and may then address another slave. After performing other tasks, the master can send a start or restart condition to the CBC92141C with a read command. The device acknowledges this request and returns the data from the register location that had previously been set up as the target.

As with the Combined Format – Read operation, the master can send a NACK and terminate the operation with a stop [P] condition, or it can send an ACK to read more data in one or more serially auto-incremented register locations.

[1] From UM10204, I²C-bus specification and user manual, Rev. 6 — 4 April 2014, NXP Semiconductor

## Hundredths Count Generation

The SC63141 generates a very approximate 100 Hz clock from the high-accuracy internal 256 Hz clock and uses this 100 Hz clock to update the hundredths- and tenths-of-a-second time register counts and to offer a 100 Hz clock option for square wave outputs and other timing features. Each cycle of the 100 Hz clock consists of 2 to 4 cycles of the 256 Hz clock. There are 4 cycles of 256 Hz in the first hundredths count period after the clock is reset (once per second). The other 99 hundredths counts consist of 2 or 3 256Hz clock cycles, alternating between 7 counts of 2 x 256Hz clock cycles and 9 counts of 3 x 256Hz clock cycles, with the exception of first set of 2 cycle counts, which includes the extra 2 cycles in the first 100th count. Except for the first cycle of each second, the resulting edge-to- edge clock jitter error is +22/-25%.

## Battery Charging

During normal operation, the CBC92141 charges the backup battery (or other energy storage device) connected to the VCHG pin, with a temperature dependent duty-cycle, frequency and charging voltage.

Upon entering normal operation (VDD rising above POR level), the CBC92141 will initially charge the backup battery for at least 72 hours and no more than 96 hours. After this initial charging duration, the SC630001 will periodically run a refresh charging operation to replenish charge lost by battery self-discharge and the leakage current from the circuit connected to the battery. These discharge effects on the battery should be very small but can accumulate over time, especially at higher temperatures, and circuit leakage currents would have a larger impact on a smaller, lower capacity battery. Accordingly, the CBC92141 has registers for the user to configure the charging frequency and to additionally configure an incrementally higher charging frequency at temperatures of +40°C or higher. This configurability enables the user to optimize the trade-offs among power draw from the primary source (at VDD), backup battery run-time, and longer backup battery life, as battery life is typically improved by leaving the battery at a lower state of charge. Also, for applications subject to large temperature changes over the course of a few days or weeks, users may prefer to configure more frequent charging cycles to correct for the effects of temperature on battery voltage. In particular, for the case that the battery is charged at a moderate or low temperature and then the temperature rises above +40C, the next charge cycle will apply the temperature compensated charging voltage and reduce the battery voltage to avoid degradation of the battery. Once a charging cycle begins, the charging frequency and charging on-time are locked in regardless of changes to the Battery Management register. However, the CHGNOW bit can be set to force a VDD POR event, which effectively reboots the charging process, including initial charging, followed by synchronization to the schedule called for in the Battery Management register.

Table 8 in the Battery Management register description section provides the charging frequencies and charger on- times corresponding to the relevant temperature ranges and the user configuration settings of the CHGFREQ and CHGTEMP register bits.

The CBC92141 uses its internal temperature measurements to adjust the voltage applied to the battery. For temperatures of 25°C or less, the charging voltage is set to VBatt. For temperatures between 25°C and 85°C, a temperature coefficient of Vbattemp_coeff is applied to reduce the charging voltage in 4°C steps to maintain good battery life. If the die temperature increases such that the temperature compensated charging voltage is less than the battery voltage, then the battery charging circuit will (during its scheduled charging on-time period) sink a small amount of current to gradually discharge the battery to the target voltage.

## Temperature Measurements and Usage

The CBC92141 includes an internal temperature measurement circuit and a 10-bit ADC to store temperature readings in the TEMPADC registers. Temperature measurements can be used by an external MCU to adjust RTC calibration parameters. The CBC92141 measures the temperature at the beginning of each charge cycle and uses this measurement to set the battery charging voltage, charger on-time, and the charging frequency time interval. This interval defines the delay until the next time that the temperature will be measured and a new charge cycle will begin. As detailed in Table **8**, the charging frequency interval can vary from 4 hours to 32 days. The MEAS_TEMP bit in a separate register can be used for external requests to update the temperature measurement. Updating the temperature measurement will update values stored in the TEMPADC registers and will immediately update the temperature-compensation of the charging voltage. However, mid-cycle temperature updates will not affect the charging frequency and charging period, which will only be updated from the temperature measurement at the beginning of the next charge cycle.

## Application Information

### VOUT Pin Capacitance

The user typically needs to place some holdup capacitance on the VOUT pin to bridge the transition into and out of backup mode. The amount of capacitance needed will depend on the application requirements according to the following equation:

$$C_{VOUT\_min} = I_{LOAD\_max} * Td_{VOUT\_rising}\ (max) / (V_{POR\_falling}\ (min) - V_{VOUT\_min})$$

Where

$I_{LOAD\_max}$ is the maximum external loading current on the VOUT bus;

$V_{VOUT\_min}$ is the minimum voltage that the application can accept at the VOUT pin during the switch-over transient;

$C_{VOUT\_min}$ is the minimum capacitance needed on the VOUT bus;

$Td_{VOUT\_rising}$ (max) is the maximum VOUT Cut-in Time delay spec. (See $Td_{VOUT\_rising}$ in Electrical Characteristics table.)

$V_{VOUT\_min}$ is the maximum external loading of the VOUT pin;

$V_{POR\_falling}$ (min) is the minimum falling VDD voltage that will trigger the CBC92141 POR function. (See $V_{POR\_falling}$ in Electrical Characteristics table.)

Note that a nominal capacitance of at least twice the minimum value is typically needed with X7* or X5* ceramic capacitors to account for capacitance variation with DC bias voltage, initial tolerance, and temperature tolerance. Check the manufacturers specifications to account for these effects.

In the case of an external power source at VOUT that provides partial support of the loading during the switch-over transient, , the minimum capacitance requirement would be reduced based on available charge from the external power source. For example, there might be a battery that is nearly drained but still has some capacity.

## Register and Memory Map

Registers are accessed by selecting a register address and then performing read or write operations. The table below lists the contents of each register. Descriptions of register variables follow later in the document. Registers are read/write type unless noted as read-only. "X"'s indicates unused registers, which return a value of zero when read.

**Color code:** RTC-only bits, PM-only bits. Contents of green highlighted registers are reset to default values on VDD mode entry.

| Offset | Reset Value | Register | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Time and Date Registers | | | | | | | | | | |
| 0x00 | 0x00 | Hundredths/Tenths | Seconds - Tenths | | | | Seconds - Hundredths | | | |
| 0x01 | 0x00 | Seconds | X | Second- Tens | | | Second-ones | | | |
| 0x02 | 0x00 | Minutes | X | Minutes- Tens | | | Minutes-ones | | | |
| 0x03 | 0x00 | Hours (24 Hr Mode) | X | X | Hours-Tens | | Hours-ones | | | |
| 0x03 | 0x00 | Hours (12 Hr Mode) | X | X | AM/ PM | Hour- Tens | Hours-ones | | | |
| 0x04 | 0x00 | Date | X | X | Date-Tens | | Date-Ones | | | |
| 0x05 | 0x00 | Months | X | X | X | Months- tens | Months-ones | | | |
| 0x06 | 0x00 | Years | Year - Tens | | | | Year-ones | | | |
| 0x07 | 0x00 | Weekdays | X | X | X | X | X | Day of Week | | |
| Alarm Registers | | | | | | | | | | |
| 0x08 | 0x00 | Hundredths/Tenths Alarm | Seconds- Alarm - Tenths | | | | Seconds Alarm- Hundredths | | | |
| 0x09 | 0x00 | Seconds Alarm | X | Seconds ALM Tens | | | Seconds ALM-ones | | | |
| 0x0A | 0x00 | Minutes Alarm | X | Minutes ALM- Tens | | | Minutes ALM-ones | | | |
| 0x0B | 0x00 | Hours Alarm (24 Hr Mode) | X | X | Hours Alarm - Tens | | Hours ALM-ones | | | |
| 0x0B | 0x00 | Hours Alarm (12 Hr Mode) | X | X | AM/P M | Hrs ALM - Tens | Hours ALM-ones | | | |
| 0x0C | 0x00 | Date Alarm | X | X | Date ALM-Tens | | Date ALM-Ones | | | |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 0x0D | 0x00 | Months Alarm | X | X | X | Months ALM-Tens | Months ALM-ones | |
| 0x0E | 0x00 | Weekdays ALM | X | X | X | X | X | Day of Week Alarm |
| 0x1C | 0x00 | RTC and OSC Control | OSEL | 12/24 | X | CENT | AOS | X |
| 0x1D | 0x00 | Stas Read Only | PSWON | 12/24 | X | CENT | AOS | X |

| Off-set | Reset Value | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| | Color coding of default (reset) values | | pre-NVM load | RTC-only version | PM-only version | full-feature version (applies to all if not otherwise specified) | | | | |
| | PM enabled trim bit | | 0 | 0 | 1 | 1 | | | | |
| | RTC enabled trim bit | | 0 | 1 | 0 | 1 | | | | |
| | color-code for register defaults | | red | blue | green | black | | | | |
| 0x0F | 0x00 | Flags (Read/Clear-Only) | SLST | XTOF | X | X | CDT | ALM | X | X |
| 0x10 | 0x00 | Access Control | STOP | X | x | x | X | X | WBATMAN | WRTC |
| 0x11 | 0x00 | Output Control | X | OUTA | OUTB | OUT2S | | | OUT1S | |
| 0x12 | 0x00 0xEC **0x02** 0xEC | Interrupt Mask | OFIE | IM | | X | CDTIE | AIE | ENPSW_WAKE | X |
| 0x13 | 0x0B (all cases) | Clock Output Control | SQWE | CLKOUT_EN | FOUT_EN | x | SQFS | | | |
| 0x14 | 0x00 | XT Calibration Configuration | XTCAL_POL | XTCAL_INIT | | | | | | |
| 0x15 | 0x00 | RC Calibration Configuration | RCCAL_POL | RCCAL_INIT | | | | | | |
| 0x16 | 0x00 | Oscillator Calibration Ranges | XTCAL_CLK | | RCCAL_CLK | X | | | | |
| 0x17 | 0x00 | Sleep Control | SLP | SLIRQ1 | SLIRQ2 | SLPORT | SLCLK | SLTO | | |
| 0x18 | 0x00 | Timer Control | CDTE | CDRPT | ALMODE | | | CDTFREQ | | |
| 0x19 | 0x00 | Countdown Timer (Read-only) | CDTIME = Countdown Timer Value | | | | | | | |
| 0x1A | 0x00 | Countdown Initial | CDTINIT = Countdown Timer Initial Value | | | | | | | |
| 0x1B | 0x80 0x80 0x09 0x09 | Charge Control | CHGOFF | CHGNOW | CHGRST | X | CHGFREQ | CHGTEMP | | |

## Register Settings

### Summary of Interrupts and Timers

Note: Flags must be cleared for respective interrupt to be re-generated on repeat timer events.

| Interrupt | Function | Interrupt Enabler | Duration | Timer Enabler | Flag |
|---|---|---|---|---|---|
| AIRQ | Alarm Match | AIE | Determined by IM (0x12 B6:B5) | ALMODE | ALM |
| TIRQ | Countdown Timer | CDTIE | Determined by IM (0x12 B6:B5) | CDTE | CDT |
| OFIRQ | Oscillator Failure | OFIE | Level held until flag is cleared | N/A | XTOF |
| IRQ | AIRQ or TIRQ or OFIRQ | | | | |

## Register Descriptions:

### Clock/Calendar Registers

Note: WRTC must be set to 1 to allow writing to clock/calendar registers 0x01-0x07

| Offset | Bits | Register | Description |
|---|---|---|---|
| 0x00 | B7:B4 | Seconds - Tenths | The tens digits of the hundredths of seconds approximation. See hundredths below. |

| | | | |
|---|---|---|---|
| 0x00 | B3:B0 | Seconds - Hundredths | - . |
| 0x001 | B7 | Not Used | |
| 0x01 | B6:B4 | Seconds - Tens | |
| 0x01 | B3:B0 | Seconds - Ones | |
| 0x02 | B7 | Not Used | |
| 0x02 | B6:B4 | Minutes - Tens | |
| 0x02 | B3:B0 | Minutes - Ones | |
| | | | |

**Minutes/Seconds Registers BCD Table**

| Decimal Time Count | | Tens | | Ones | | | |
|---|---|---|---|---|---|---|---|
| | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| . . . | | | | | | | |
| 9 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 10 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 11 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 12 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 13 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| . . . | | | | | | | |
| 57 | 1 | 0 | 1 | 0 | 1 | 1 | 1 |
| 58 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 59 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |

| | | |
|---|---|---|
| 0x03 | B7:B6 | Not Used |
| 0x03 | B5:B4 | Hours-Tens (24-hour mode) |
| 0x03 | B5 | AM/PM (12-hour mode) |
| 0x03 | B6 | Hours-Tens (12-hour mode) |
| 0x03 | B3:B0 | Hours-ones (12-hour and 24-hour modes) |

**24-Hour Mode**

| 24-hour count | Hours-Tens | | Hours-Ones | | | |
|---|---|---|---|---|---|---|
| | B5 | B4 | B3 | B2 | B1 | B0 |
| | 20 | 10 | 8 | 4 | 2 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 0 | 0 | 1 | 0 |
| . . . | | | | | | |
| 9 | 0 | 0 | 1 | 0 | 0 | 1 |
| 10 | 0 | 1 | 0 | 0 | 0 | 0 |
| 11 | 0 | 1 | 0 | 0 | 0 | 1 |
| 12 | 0 | 1 | 0 | 0 | 1 | 0 |
| 13 | 0 | 1 | 0 | 0 | 1 | 1 |
| . . . | | | | | | |
| 19 | 0 | 1 | 1 | 0 | 0 | 1 |
| 20 | 1 | 0 | 0 | 0 | 0 | 0 |
| 21 | 1 | 0 | 0 | 0 | 0 | 1 |
| 22 | 1 | 0 | 0 | 0 | 1 | 0 |
| 23 | 1 | 0 | 0 | 0 | 1 | 1 |

**12-hour mode**

| 12-hour count | AM/PM | Hours-Tens | Hours-Ones | | | |
|---|---|---|---|---|---|---|
| | | B4 | B3 | B2 | B1 | B0 |
| | | 10 | 8 | 4 | 2 | 1 |
| 12 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 0 | 0 | 1 | 0 |
| . . . | | | | | | |
| 9 | 0 | 0 | 1 | 0 | 0 | 1 |
| 10 | 0 | 1 | 0 | 0 | 0 | 0 |
| 11 | 0 | 1 | 0 | 0 | 0 | 1 |
| 12 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| | | | | | | |
| 7 | 0 | 0 | 0 | 1 | 1 | 1 |
| 8 | 0 | 0 | 1 | 0 | 0 | 0 |
| 9 | 0 | 0 | 1 | 0 | 0 | 1 |
| 10 | 0 | 1 | 0 | 0 | 0 | 0 |
| 11 | 0 | 1 | 0 | 0 | 0 | 1 |

| | | |
|---|---|---|
| 0x04 | B7:B6 | Not Used |
| 0x04 | B5:B4 | Date (Tens) |
| 0x04 | B3:B0 | Date (Ones) |

**Days Register BCD Table**

| | Tens | | Ones | | | |
|---|---|---|---|---|---|---|
| Date | B5 | B4 | B3 | B2 | B1 | B0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 0 | 0 | 1 | 0 |
| . . . | | | | | | |
| 9 | 0 | 0 | 1 | 0 | 0 | 1 |
| 10 | 0 | 1 | 0 | 0 | 0 | 0 |
| 11 | 0 | 1 | 0 | 0 | 0 | 1 |
| 12 | 0 | 1 | 0 | 0 | 1 | 0 |
| 13 | 0 | 1 | 0 | 0 | 1 | 1 |
| . . . | | | | | | |
| 26 | 1 | 0 | 0 | 1 | 1 | 0 |
| 27 | 1 | 0 | 0 | 1 | 1 | 1 |
| 28 | 1 | 0 | 1 | 0 | 0 | 0 |
| 29 | 1 | 0 | 1 | 0 | 0 | 1 |
| 30 | 1 | 1 | 0 | 0 | 0 | 0 |
| 31 | 1 | 1 | 0 | 0 | 0 | 1 |

| | | |
|---|---|---|
| 0x05 | B7:B5 | Not Used |
| 0x05 | B4 | Months-tens |
| 0x05 | B3:B0 | Months-ones |

**Months Register BCD Table**

| Month | Tens | | Ones | | | |
|---|---|---|---|---|---|---|
| | B5 | B4 | B3 | B2 | B1 | B0 |
| | 20 | 10 | 8 | 4 | 2 | 1 |
| January | 0 | 0 | 0 | 0 | 0 | 1 |
| February | 0 | 0 | 0 | 0 | 1 | 0 |
| March | 0 | 0 | 0 | 0 | 1 | 1 |
| April | 0 | 0 | 0 | 1 | 0 | 0 |
| May | 0 | 0 | 0 | 1 | 0 | 1 |
| June | 0 | 0 | 0 | 1 | 1 | 0 |
| July | 0 | 0 | 0 | 1 | 1 | 1 |
| August | 0 | 0 | 1 | 0 | 0 | 0 |
| September | 0 | 0 | 1 | 0 | 0 | 1 |
| October | 0 | 1 | 0 | 0 | 0 | 0 |
| November | 0 | 1 | 0 | 0 | 0 | 1 |
| December | 0 | 1 | 0 | 0 | 1 | 0 |

<table>
<tr><td>0x06</td><td>B7:B4</td><td>Years-tens</td><td rowspan="2">
<table>
<tr><th colspan="9">Years Register BCD Table</th></tr>
<tr><th></th><th colspan="4">Years-Tens</th><th colspan="4">Hours-Ones</th></tr>
<tr><th></th><th>B7</th><th>B6</th><th>B5</th><th>B4</th><th>B3</th><th>B2</th><th>B1</th><th>B0</th></tr>
<tr><th></th><th>80</th><th>40</th><th>20</th><th>10</th><th>8</th><th>4</th><th>2</th><th>1</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>2</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>. . .</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>9</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>10</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>11</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>12</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>13</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>. . .</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>19</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>20</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>21</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>22</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>23</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>24</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>. . .</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>96</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>97</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>98</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>99</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td></tr>
</table>
</td></tr>
<tr><td>0x06</td><td>B3:B0</td><td>Years-ones</td></tr>
<tr><td>0x07</td><td>B2:B0</td><td>Day of Week</td><td>The 3 day of week register bits comprise a numerical count from 0 to 6 that increments by 1 every 24 hours and then returns to 0 when incrementing from 6. As with the other calendar or clock registers, the user can write a value to this register via the serial port to synchronize it with a preferred calendar system. For example, the user can choose to have 000 represent Sunday or Monday.</td></tr>
</table>

## Alarm Registers 0x08-0x0E

| | | | |
|---|---|---|---|
| 0x08-0x0E | | Alarm Registers | The data in the alarm registers are organized in the same way as shown above for the time and date registers 0x00-0x07. These registers are written by the host software to set the time and date for the alarm event which occurs when the data in the selected alarm registers (selected by ALMODE) match the corresponding data in the time and date registers. |

## Flag Register 0x0F (Read/Clear-Only)

These bits are cleared when this register is read through the serial port. Exception: SLST will not be cleared while SLEEP=1. These bits cannot be set from the serial port. Timer flags (ALM and CDT) must be cleared (by reading) for respective timer event recurrences to trigger an interrupt. Periodic reading of flags may be advised in case an interrupt was not serviced, and especially upon entering VDD mode in case of latent interrupts generated during backup mode operation.

| | | | |
|---|---|---|---|
| 0x0F | B7 | SLST | The CBC92141 sets this bit to 1 when it engages the sleep state (after the sleep timer reaches 0.) This bit is NOT automatically reset by the CBC92141. (See SLEEP bit in the status register which is also set to 1 when engaging the sleep state but is automatically reset when an interrupt terminates the sleep state.) This bit is left set to a value of 1 as a record that the system has been in the sleep state. The external software should reset this bit prior to setting the SLP bit for the next sleep period. This bit cannot be cleared while in the sleep state (while SLEEP=1). |
| 0x0F | B6 | XTOF | Crystal Oscillator failure flag. The I.C. sets this bit to 1 after an unsuccessful attempt to switch its clock source from the RC oscillator to the crystal oscillator. |
| 0x0F | B5:B4 | NOT USED | |
| 0x0F | B3 | CDT | The CBC92141 sets this bit to 1 when the TE=1 and the Countdown Timer reaches zero. Flag must be cleared (by reading) for countdown timer event recurrence to trigger an interrupt. |
| 0x0F | B2 | ALM | this bit to 1 when the alarm registers selected by ALMODE match the corresponding time and date registers. |
| 0x0F | B1:B0 | NOT USED | |

## Control Registers 0x10-0x11

| | | | |
|---|---|---|---|
| 0x10 | B7 | STOP | Setting this bit to 1 stops the incrementing of the time and date registers. While this bit is set at least some of the selectable clock outputs may be disabled. Resetting the STOP bit to 0 resumes the incrementing of the time and date registers. Setting STOP to 1 allows the system to write 0 or other desired values to the time and date counters and then restart the counting at a particular time by resetting this bit to 0. Since the battery charging schedule utilizes the RTC registers, while STOP=1, battery charging will be extended if the charger is on or delayed if the charger is off. This bit cannot be written unless WRTC=1. |
| 0x10 | B6:B2 | NOT USED | |
| 0x10 | B1 | WBATMAN | Write Battery Management. This bit must be set to 1 in order to write to the Battery Management Register (CHGFREQ, CHGTEMP, and BCMFREQ) or the Charge Control Register (CHGOFF, CHGNOW, and CHGRST). |

| | | | |
|---|---|---|---|
| 0x10 | B0 | WRTC | Write RTC. This bit must be set in order to write the STOP bit, CENT bit, or any of the Counter registers (Hundredths, Seconds, Minutes, Hours, Date, Months, Years or Weekdays). Writing to the RTC registers can affect the battery charging schedule and may even cause a charge cycle to be missed if the charging start time is skipped due to a change of the time. It might be useful to set the CHGNOW bit in this case. |
| 0x11 | B7 | NOT USED | |
| 0x11 | B6 | OUTA | This is a static value which may be driven on the nPGD/nIRQ pin, depending on the OUT1S setting. If the OUTA value is selected by OUT1S, a value of 0 pulls the nPGD/nIRQ pin low; whereas a value of 1 leaves this pin open drain. |
| 0x11 | B5 | OUTB | This is a static default value which may be driven on the PSW/nIRQ2 pin, depending on the OUT2S and ENPSW_WAKE settings. If the OUTB value is selected by OUT2S and enabled by ENPSW_WAKE, a value of 0 pulls the PSW/nIRQ2 pin low using the internal low-resistance switch; whereas a value of 1 leaves this pin open drain, which could disconnect power to external components if the PSW/nIRQ2 pin is being used as a power switch. |
| 0x11 | B4:B2 | OUT2S | Selects the function of the nIRQ2 pin based on Table 1, assuming both logic states are allowed by ENPSW_WAKE when not in SLEEP. |
| 0x11 | B1:B0 | OUT1S | Selects the function of the nPGD/nIRQ pin based on Table 2. |

**Table 1: Functions of PWS/nIRQ2 pin determined by OUT2S Register Bits**

| 0x11 B4 | 0x11 B3 | 0x11 B2 | Hex value of 0x11 B4:B2 (OUT2S) | PSW/nIRQ2 Pin Function (NOTE: logic low output is forced if ENPSW_WAKE=SLEEP=0 or SLEEP=nSLIRQ2=1) |
|---|---|---|---|---|
| **0** | **0** | **0** | **x0** | **nIRQ if at least one interrupt is enabled, else nCHGON (default)** |
| 0 | 0 | 1 | x1 | SQW if enabled by SQWE=1, else OUTB |
| 0 | 1 | 0 | x2 | AIRQ if AIE is set, else OUTB |
| 0 | 1 | 1 | x3 | nAIRQ if AIE is set, else OUTB |
| 1 | 0 | 0 | x4 | TIRQ if CDTIE is set, else OUTB |
| 1 | 0 | 1 | x5 | nTIRQ if CDTIE is set, else OUTB |
| 1 | 1 | 0 | x6 | SLEEP AND SLIRQ2 |
| 1 | 1 | 1 | x7 | OUTB |

**Table 2: Functions of nPGD/nIRQ pin determined by OUT1S Register Bits**

| 0x11 B1 | 0x11 B0 | Hex value of 0x11 B1:B0 OUT1S | nPGD/nIRQ Pin Function |
|---|---|---|---|
| **0** | **0** | **x0** | **nPGOOD (default)** |
| 0 | 1 | x1 | SQW if enabled by SQWE=1 and FOUT_EN =1, else CAL64 |
| 1 | 0 | x2 | nIRQ if at least one interrupt is enabled, else OUTA |
| 1 | 1 | x3 | nAIRQ if AIE is set, else OUTA |

## Interrupt Mask Register 0x12

| | | | |
|---|---|---|---|
| 0x12 | B7 | OFIE | (XT) Oscillator Fail interrupt enable. When 1, an Oscillator Failure will generate an OFIRQ signal. An XT oscillator failure would be detected when switching from the RC to the XT oscillator upon request. |
| 0x12 | B6:B5 | IM | Interrupt Mode. This value controls the duration of the interrupt signals AIRQ and TIRQ. Options are shown in Table 3. |
| 0x12 | B4 | NOT USED | |
| 0x12 | B3 | CDTIE | Timer Interrupt Enable. When this bit is set to 1, the Countdown Timer will generate a TIRQ interrupt signal and set the CDT flag when the timer count reaches 0. |

| | | | |
|---|---|---|---|
| 0x12 | B2 | AIE | Alarm Interrupt Enable. When this bit is set to 1, and all selected alarm registers (selected by ALMODE in the Timer register) match the corresponding time/date registers, the SC63141 will generate an AIRQ interrupt signal. |
| 0x12 | B1 | ENPSW_WAKE | A value of 1 enables the logic functions selected by OUT2S. A value of zero overrides any other selections to keep the low resistance switch on (active low output) at the PSW/nIRQ1 pin while SLEEP=0. If using this pin as a power switch to cut off the ground return of one of more external devices when SLEEP=1 (per the configuration shown in Figure 17), set this bit to zero as a precaution to prevent power cut-off from occurring outside of the SLEEP state. |
| 0x12 | B0 | NOT USED | |

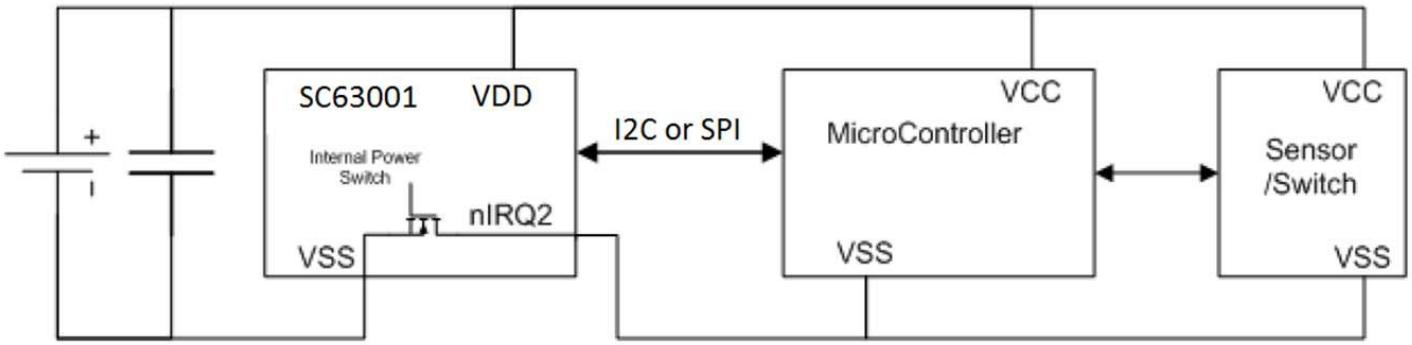



**Figure 8: Switched ground configuration optionally used to disconnect power from external devices during SLEEP**

**Table 3: Alarm Interrupt signal duration as determined by setting of IM register bits**

| 0x12 B1 | 0x12 B0 | Hex value of 0x12 B6:B5 (IM) | Alarm Interrupt Signal (nAIRQ, nAIRQ2) Duration |
|---|---|---|---|
| 0 | 0 | x0 | Continuous for both XT mode and RC mode (until interrupt flag is cleared) |
| 0 | 1 | x1 | 1/256 second |
| 1 | 0 | x2 | 1/64 second |
| **1** | **1** | **x3** | **1/4 second (default)** |

## Clock Output Control Register 0x13

| | | | |
|---|---|---|---|
| 0x13 | B7 | SQWE | Square Wave Enable. Setting this bit to 1 enables the square wave output. Other bits control the application of the square wave output to CBC92141 output pins. When this bit has a value of 0, the square wave output is held at the value of OUTA. |
| 0x13 | B6 | CLKOUT_EN | A value of 1 connects the square wave output to the CMOS CLKOUT pin. A value of 0 causes the CLKOUT pin to indicate whether charging is currently disabled by CHGOFF or CHGRST. |
| 0x13 | B5 | FOUT_EN | A value of 1 connects the square wave output to the open drain nPGD/nIRQ pin if OUT1S=01 and SQWE=1. |
| 0x13 | B4 | NOT USED | |
| 0x13 | B3:B0 | SQFS | Selects the frequency of the square wave output according to Table 4. A value of 0001 selects the oscillator frequency, either 32.768 kHz if an XT is utilized or 256 Hz if the RC oscillator is selected. To avoid glitches on any output clock signals when changing the square wave output frequency selection, SQWE or one of the output control bits (OUT1S, OUT2S, CLKOUT_END, or FOUT_EN) should be temporarily changed to disable the square wave output at any of the corresponding pins. |

**Table 4: Square Wave Output Frequency vs. SQFS Register Setting**

| 0x13 B3 | 0x13 B2 | 0x13 B1 | 0x13 B0 | Hex value of 0x24 B3:B0 | Square Wave Output Frequency | Conditions/Comments |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | x0 | 100 Hz (approximate) | Approximation derived from 256 Hz clock (see description of hundredths generation.) |
| 0 | 0 | 0 | 1 | x1 | 32.768 kHz | in XT mode only, logic low otherwise |
| 0 | 0 | 1 | 0 | x2 | 1 year | Low duty cycle (<<50%), non-periodic due to leap years |
| 0 | **0** | **1** | **1** | x3 | 1 month | Low duty cycle (<<50%), non-periodic due to months |
| 0 | 1 | 0 | 0 | x4 | 1 day | |
| 0 | 1 | 0 | 1 | x5 | 1 hour | |
| 0 | 1 | 1 | 0 | x6 | 1 minute | |
| 0 | 1 | 1 | 1 | x7 | 256 Hz | |
| 1 | 0 | 0 | 0 | x8 | 128 Hz | |
| 1 | 0 | 0 | 1 | x9 | 64 Hz | |
| 1 | 0 | 1 | 0 | xA | 32 Hz | |
| 1 | **0** | **1** | **1** | **xB** | **16 Hz** | **Default value** |
| 1 | 1 | 0 | 0 | xC | 8 Hz | |
| 1 | 1 | 0 | 1 | xD | 4 Hz | |
| 1 | 1 | 1 | 0 | xE | 2 Hz | |
| 1 | 1 | 1 | 1 | xF | 1 Hz | |

## Real-Time Clock Calibration Registers: 0x14-0x16

A configurable calibration scheme in the CBC92141 accounts for oscillator inaccuracy by making corrections to the time keeping. The user can select separate parameters for RC and crystal oscillator modes. Pulses are added or skipped in the 64 Hz clock at user-configurable calibration intervals, depending on the setting of the RCCAL_POL or XTCAL_POL value. Only downstream (lower frequency) clocks and registers, not including any bits of the tenths/hundredths register, are affected by this calibration process. The calibration interval is determined by a 7-bit Calibration Interval Timer Counter which loads an initial value (XTCAL_INIT or RCCAL_INIT) at the beginning of each calibration interval and counts down to zero, at which time the 64 Hz clock adjustment is made, and the initial value is reloaded into the counter. Selectable clock inputs to this timer, XTCAL_CLK or RCCAL_CLK, provide for wide ranges of calibration in each of the oscillator modes to accommodate the tolerances of the external crystal or the internal RC oscillator. Once the Calibration Interval Timer Counter begins to count down, updates to the associated initial value, polarity, or clock parameters do not take effect until the next calibration cycle. The block diagram in Figure 7 below illustrates the operation of the oscillator calibration.

| | | | |
|---|---|---|---|
| 0x14 | B7 | XTCAL_POL | Calibration polarity for crystal oscillator mode. A value of 1 causes each RTC calibration action to add a pulse to the 64 Hz clock when the oscillator is in XT oscillator mode (OMODE=1) to compensate for a slow crystal. A value of zero results in a skipped pulse to compensate for a fast crystal. |
| 0x14 | B6:B0 | XTCAL_INIT | Calibration timer initial value for crystal oscillator mode. This value is reloaded into the Calibration Interval Timer Counter after each calibration event when the oscillator is in XT oscillator mode (OMODE=1). When the counter reaches zero a positive or negative adjustment is made to the 64 Hz clock, depending on the XTCAL_POL setting. Set this value to zero to disable RTC calibration while operating from the crystal oscillator. |
| 0x15 | B7 | RCCAL_POL | Calibration polarity for RC oscillator mode. A value of 1 causes each RTC calibration action to add a pulse to the 64 Hz clock when the oscillator is in RC oscillator mode (OMODE=0) to compensate for a slow crystal. A value of zero results in a skipped pulse to compensate for a fast crystal. |
| 0x15 | B6:B0 | RCCAL_INIT | Calibration timer initial value for RC oscillator mode. This value is reloaded into the Calibration Interval Timer Counter after each calibration event when the oscillator is in RC oscillator mode (OMODE=0). When the counter reaches zero a positive or negative adjustment is made to the 64 Hz clock, depending on the RCCAL_POL setting. Set this value to zero to disable RTC calibration while operating from the RC oscillator. |
| 0x16 | B7:B6 | XTCAL_CLK | Calibration timer clock selection for crystal oscillator mode. **Table** 5 shows the frequency selections (actually time intervals) selected by this register value. This selection determines the clock rate at which the Calibration Interval Timer Counter is decremented in XT oscillator mode. This selection trades off calibration range and resolution, as a larger value provides for less frequent corrections, as desired for a crystal with good initial accuracy. |
| 0x16 | B5 | RCCAL_CLK | Calibration timer clock selection for RC oscillator mode. **Table** 5 shows the frequency selections selected by this register value. This selection determines the clock rate at which the Calibration Interval Timer Counter is decremented in RC oscillator mode. This selection trades off calibration range and resolution, as a larger value provides for less frequent corrections. |
| 0x16 | B4:B0 | NOT USED | |

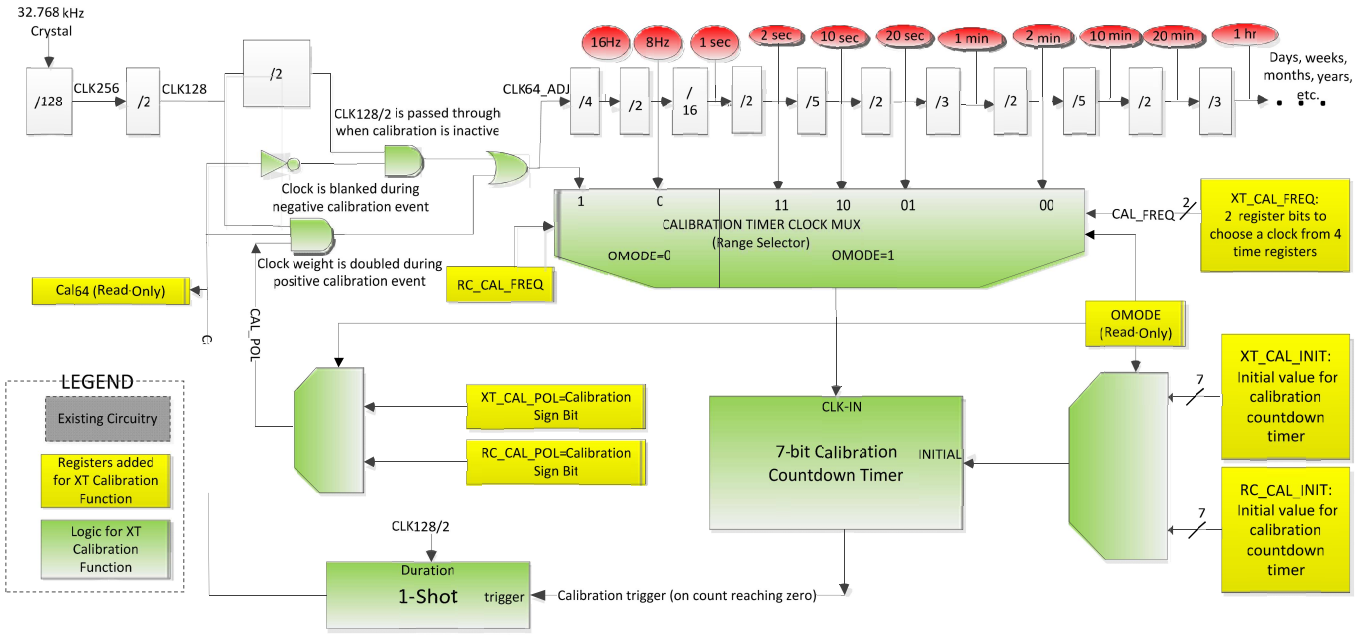



**Figure 7: Block diagram for oscillator calibration functionality. Yellow blocks are registers.**

**Table 5: Calibration timer clock selections as determined by 0x16 B7:B5 and OMODE (0x1D B4)**

| 0x16 B7 | 0x16 B6 | 0x16 B5 | 0x1D B4 (OMODE) | Clock frequency for Calibration Counter (Tmin=Minimum Calibration Interval) | Maximum Calibration Interval (Tmax) | Max. PPM Adjustment (at Tmin) | Min. PPM Adjustment (at Tmax) | PPM Resolution (at Tmax) |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | x | 1 | 120 sec | 15360 sec | 65 | 1.0 | 0.008 |
| 0 | 1 | x | 1 | 20 sec | 2560 sec | 391 | 6.2 | 0.05 |
| 1 | 0 | x | 1 | 10 sec | 1280 sec | 781 | 12.3 | 0.10 |
| 1 | 1 | x | 1 | 2 sec | 256 sec | 3906 | 61.5 | 0.49 |
| x | x | 0 | 0 | 16 Hz | 8 sec | 125000 | 1968 | 15.6 |
| x | x | 1 | 0 | 64 Hz | 2 sec | 500000 | 7874 | 62.5 |

## Sleep Control Register 0x17

See the state diagram of Figure 19 for an overview of the sleep state controller.

| | | | |
|---|---|---|---|
| 0x17 | B7 | SLP | Sleep request. Setting this value to 1 initiates the pre-sleep timer, which counts down to imposition of the sleep state onto one or more external devices. The SLP bit will be cleared when the sleep state is terminated by any of the interrupts (IRQ=1) . In order to ensure a wake-up means before sleeping, this bit can only be set to 1 if STOP=0 (counters enabled) and one of the wake-up timers (alarm or countdown timer) is set with its associated interrupt enabled, and all interrupt flags have been reset to zero. Depending on the sleep I/O settings (SLPORT, SLIRQ1, SLIRQ2, and SLCLK) , I/O's maybe unavailable while SLP=1. If a floating state (due to use of the PSW/nIRQ2 to disconnect power) is specified by these bits for any of the CBC92141 outputs, then those outputs will be driven high in the SLEEP state and (except for the PSW/nIRQ2 in) may begin transitioning once SLP is set to 1. |
| 0x17 | B6 | SLIRQ1 | User-selected sleep setting for the nPGD/nIRQ output pin. A value of 0 results in an open-drain state on the nPGD/nIRQ pin in the sleep state (when SLEEP=1). A value of 1 allows the OUT1S logic to determine the state of the nPGD/nIRQ pin, even during the sleep state. |
| 0x17 | B5 | SLIRQ2 | User-selected sleep state setting of the PSW/nIRQ2 output pin. This value affects the logic level of the PSW/nIRQ2 output pin in the sleep state. A value of 0 results in an active low state during sleep. A value of 1 allows the OUT2S logic to determine the state of this open-drain output pin when SLEEP=1 . SLIRQ2 should be set to 1 if the application configuration uses the PSW/nIRQ2 pin to directly disconnect power (i.e., ground/VSS return line) to external components during the sleep state per the configuration of Figure 17. |
| 0x17 | B4 | SLPORT | User-selected sleep state setting of the serial port. This bit should be set to 1 only if the serial port will be used during the sleep state. This bit MUST be set to 0 if the serial port is connected to a device that will be floating during the sleep state, for example, due to the PSW/nIRQ2 disconnection of the ground return line. While SLPORT is set to 0 and SLP is set to 1, the serial port will be unavailable for communications. |

| | | | |
|---|---|---|---|
| 0x17 | B3 | SLCLK | Sleep state of CLKOUT pin. A value of 0 disables the clock output function of the CLKOUT pin and forces this pin high in the sleep state (SLEEP=1). Use this setting if CLKOUT will be connected to the input of a floating MCU device during the sleep state (for example, if using the PSW/nIRQ2 pin to disconnect the ground of the MCU). A value of 1 allows full function of the CLKOUT pin during the sleep state. |
| 0x17 | B2:B0 | SLTO | Pre-sleep timer setting. This sets the number of 7.8 ms (128 Hz) periods after SLP is set until the CBC92141 engages the sleep state. If SLTO and SLSORT are both set to 0, a 3.4 ms (1/256 sec) delay will be added before the sleep state is engaged; this gives the CBC92141 time to prepare the serial port for the possibility that the I/O's will be floating in the sleep state. |

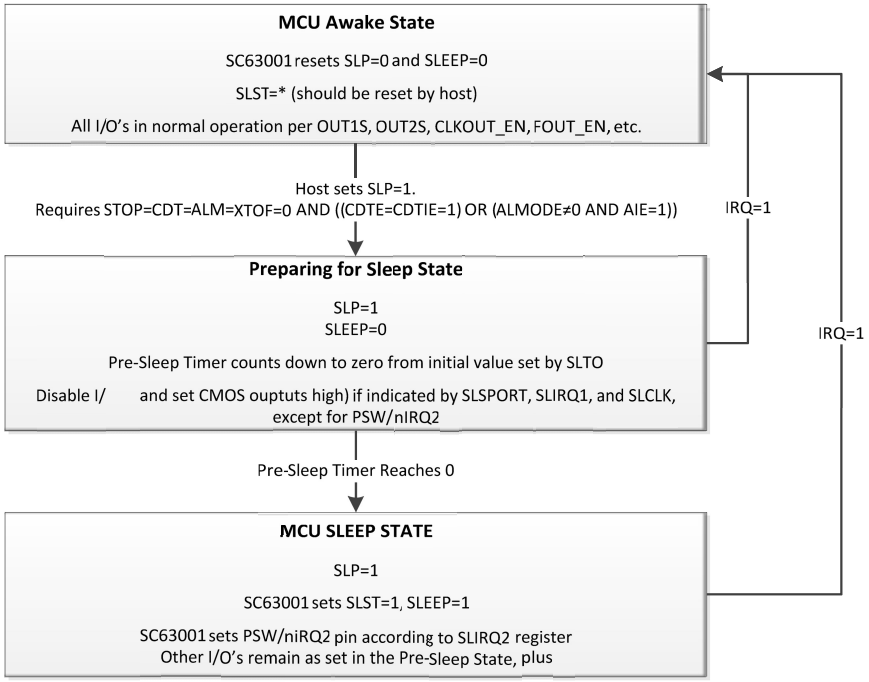



**Figure 8: State diagram representing the sleep state controller and associated features**

## Timer Management Registers 0x18-0x1A

| | | | |
|---|---|---|---|
| 0x18 | B7 | CDTE | Countdown Timer Enable. A value of 1 enables decrementing in the Countdown Timer, as reported in the Countdown Timer register. Disabling the timer with a value of 0 stops the countdown but retains the latest value in the Countdown Timer register. |
| 0x18 | B6 | CDRPT | Countdown Timer Repeat. With a value of 1, when the Countdown Timer reaches zero, it reloads the value of the Timer Initial Value register into the Countdown Timer register and begin another countdown. A value of 0 causes the Countdown Timer to stop after reaching zero. This value should be toggled to 1 in order to load the CDTINIT value when starting the Countdown Timer. It can be reset to zero after loading if the repeat function is not desired. |
| 0x18 | B5:B2 | ALMODE | Alarm mode selection and enabling. This selection determines which bits of the Alarm registers are considered for determining a match that will set off the Alarm interrupt. The options are shown in Table 7. Several options, including the zero (x0) value, disable the alarm. |
| 0x18 | B1:B0 | CDTFREQ | Countdown Timer frequency selection according to Table 7. This frequency determines the clock rate at which the countdown timer is decremented. |
| 0x19 | B7:B0 | CDTIME (Read-only) | Countdown Timer Value. Current value of the countdown timer. When the Countdown Timer is enabled (CDTE=1) and the value of this register is non-zero, this value is decremented one LSB for each cycle of the frequency selected by CDTFREQ. The remaining countdown time is equal to the Countdown Timer Value divided by the Countdown Frequency. |
| 0x1A | B7:B0 | CDTINIT | Countdown Timer Initial Value. This value is loaded into the Countdown Timer (CDTIME) register when CDTIME=0 and CDRPT= 1. |

**Table 6: Alarm modes determined by ALMODE. X indicates alarm register selected for match detection**

| 0x18 B5 | 0x18 B4 | 0x18 B3 | 0x18 B2 | Hex value of 0x18 B5:B2 | Alarm Frequency | months | date | weekdays | hours | minutes | seconds | Tenths | Hundredths (B3:B0) | Comment |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **0** | **0** | **0** | **0** | **x0** | **Alarm Disabled** | | | | | | | | | **Default setting** |
| 0 | 0 | 0 | 1 | x1 | yearly | X | X | | X | X | X | X | X | |
| 0 | 0 | 1 | 0 | x2 | monthly | | X | | X | X | X | X | X | |
| 0 | 0 | 1 | 1 | x3 | weekly | | | X | X | X | X | X | X | |
| 0 | 1 | 0 | 0 | x4 | daily | | | | X | X | X | X | X | |
| 0 | **1** | **0** | **1** | **x5** | Hourly | | | | | X | X | X | X | |
| 0 | 1 | 1 | 0 | x6 | 1 minute | | | | | | X | X | X | |
| 0 | 1 | 1 | 1 | x7 | 1 Hz | | | | | | | X | X | |
| 1 | 0 | 0 | 0 | x8 | 10 Hz | | | | | | | | X | Subject to inexact hundredths counter |
| | | | | X9-xF | Invalid states | | | | | | | | | Disables alarm, but x0 is preferred setting to disable. |

**Table 7: Countdown Timer frequency settings for CDTFREQ values**

| CDTFREQ bits | | Countdown Frequency |
|---|---|---|
| **0x18 B1** | **0x18 B0** | |
| 0 | 0 | 256 Hz |
| 0 | 1 | 1 Hz |
| 1 | 0 | 1/60 Hz (once per minute) |
| 1 | 1 | 1/3600 Hz (once per hour) |

## Charging Control Register 0x1B

Note: The WBATMAN register must be set to 1 in order to allow updating of this register.

| | | | |
|---|---|---|---|
| 0x1B | B7 | CHGOFF | Charger off. Setting this bit to 1 inhibits battery charging. Temporary shutdown of the battery charger could be useful for conserving limited system power in some situations. The charging schedule will run in the background but charging will not occur while CHGOFF=1. Setting CHGNOW to 1 resets CHGOFF to zero. This bit is also reset to the default value of zero when the CBC92141 comes out of battery backup mode. To prevent battery charging, this bit would need to be set back to 1 after serial communications resume with VDD operation. WBATMAN must equal 1 to allow updating of this bit. |
| 0x1B | B6 | CHGNOW | Charge now. Toggling this bit from 0 to 1 causes the CBC92141 to reset the CHGOFF and CHGRST bits to 0 (if not already equal to zero) and perform a VDD power-on-reset, the main effect being that it forces an initial charge cycle and then synchronizes the charging schedule to the latest CHGFREQ and CHGTEMP values. This function is particularly useful in case low values of CHGFREQ (long charging frequency intervals) are being used and a sustained substantial increase in the ambient temperature is observed. The user needs to reset this CHGNOW bit to 0 in order to use this feature again. WBATMAN must equal 1 to allow updating of this bit. |
| 0x1B | B5 | CHGRST | Resets the charging controller to its idle state where it is waiting for the next charging period clock edge. Once CHGRST is set back to zero the charging controller will again start to look for the rising edge of the charging period clock and subsequently begin the charging cycle. This bit is reset to the default value of zero when the CBC92141 comes out of battery backup mode. Setting CHGNOW to 1 also resets CHGRST to zero. WBATMAN must equal 1 to allow updating of this bit. |
| 0x1B | B4 | NOT USED | |

| | | | |
|---|---|---|---|
| 0x1B | B3:B2 | CHGFREQ | Charging Frequency. These 2 bits configure the frequency of the backup battery charger cycling. A value of 00 gives the least frequent charging. Higher values increase the frequency of the charging operation. The on-times of the charger scale approximately with the charging period (1/frequency) and these on-times are reduced for successively higher temperature ranges. (See Table 9 and explanation of CHGTEMP register bits for behavior above 40°C.) WBATMAN must equal 1 to allow updating of these bits. |
| 0x1B | B1:B0 | CHGTEMP | Temperature compensation of charging frequency. These 2 bits configure the increase of charging frequency at temperatures above 40°C relative to the setting of the CHGFREQ bits. A CHGTEMP value of 00 results in a fixed charging frequency, as set by the CHGFREQ bits. For higher values of CHGTEMP, each incremental value increases the frequency of the charging operation above 40°C. The charging frequencies and on-times are listed in Table 8 for the full temperature range and the possible combinations CHGFREQ and CHGTEMP. WBATMAN must equal 1 to allow updating of these bits. |

**Table 8:Charging Times and Frequencies for full temperature range vs. CHGFREQ and CHGTEMP values.**

| CHGFREQ | | CHGTEMP | | hex code | Nominal Charging Frequency | | Nominal Charger On-Time vs. Temperature | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x1B B3 | 0x1B B2 | 0x1B B1 | 0x1B B0 | of B3:B0 | below 40°C | above 40°C | Temp < -20°C | -20°C to 0°C | 0°C to 40°C | Temp > 40°C |
| 0 | 0 | 0 | 0 | x0 | 32 days | 32 days | 8 days | 4 days | 1 day | 8 hours |
| 0 | 0 | 0 | 1 | x1 | 32 days | 8 days | 8 days | 4 days | 1 day | 2 hours |
| 0 | 0 | 1 | 0 | x2 | 32 days | 4 days | 8 days | 4 days | 1 day | 1 hour |
| 0 | 0 | 1 | 1 | x3 | 32 days | 2 days | 8 days | 4 days | 1 day | 20 minutes |
| 0 | 1 | 0 | 0 | x4 | 8 days | 8 days | 2 days | 1 day | 8 hours | 2 hours |
| 0 | 1 | 0 | 1 | x5 | 8 days | 4 days | 2 days | 1 day | 8 hours | 1 hour |
| 0 | 1 | 1 | 0 | x6 | 8 days | 2 days | 2 days | 1 day | 8 hours | 20 minutes |
| 0 | 1 | 1 | 1 | x7 | 8 days | 1 day | 2 days | 1 day | 8 hours | 20 minutes |
| 1 | 0 | 0 | 0 | x8 | 4 days | 4 days | 1 day | 1 day | 4 hours | 1 hour |
| **1** | **0** | **0** | **1** | **x9 *** | **4 days** | **2 days** | **1 day** | 1 day | **4 hours** | **20 minutes** |
| 1 | 0 | 1 | 0 | xA | 4 days | 1 day | 1 day | 1 day | 4 hours | 20 minutes |
| 1 | 0 | 1 | 1 | xB | 4 days | 8 hours | 1 day | 1 day | 4 hours | 4 minutes |
| 1 | 1 | 0 | 0 | xC | 2 days | 2 days | 1 day | 8 hours | 2 hours | 20 minutes |
| 1 | 1 | 0 | 1 | xD | 2 days | 1 day | 1 day | 8 hours | 2 hours | 20 minutes |
| 1 | 1 | 1 | 0 | xE | 2 days | 8 hours | 1 day | 8 hours | 2 hours | 4 minutes |
| 1 | 1 | 1 | 1 | xF | 1 days | 4 hours | 8 hours | 4 hours | 1 hour | 4 minutes |

*** Default value is in bold**.

## Oscillator and RTC Configuration Registers 0x1C

| | | | |
|---|---|---|---|
| 0x1C | B7 | OSEL | A value of 0 requests the RC Oscillator to generate a 256Hz clock for the timer circuits. A value of 1 requests the XT Oscillator to generate a 32.786 kHz clock which is divided down to 256 Hz for the timer circuit. Upon transitioning from 0 to 1, the XT oscillator will first be checked against the RC oscillator to ensure XT operation prior to changing the clock source. If the XT oscillator functional check is not satisfied, the CBC92141 will reset OSEL to zero and continue operating from the RC oscillator. |
| 0x1C | B6 | 12_24 | A value of 0 selects 24 hour mode operation of the hours register. A value of 1 selects 12 hour mode. Changing this bit does NOT change the Hours Alarm register. It is recommended that the Hours Alarm register value be set by the user based on the mode selected by this bit. |
| 0x1C | B5 | CENT | Century indicator for the calendar. This bit may be written via the serial port while WRTC=1. It automatically toggles when the calendar year register transitions from 99 back to 00 . A value of 1 results in calendar counting with century 20xx leap years, and a value of 0 results in counting with century 210x leap years (same as 19xx). |
| 0x1C | B4 | AOS | A value of 1 enables automatic switch over to the RC oscillator upon the CBC92141 entering backup mode. If OSEL=1, the CBC92141 will revert to the XT oscillator upon returning to VDD mode. An AOS value of 0 disables automatic oscillator switch over. |
| 0x1C | B3:B0 | NOT USED | |

## Status Register 0x1D (Read-Only)

| | | | |
|---|---|---|---|
| 0x1D | B7 | PSWON | A value of 1 indicates that the low-resistance internal switch at the PSW/nIRQ2 pin is on. A value of 0 indicates that this pin is in an open-drain state. |
| 0x1D | B6 | CAL64 | This value is high while the RTC calibration circuit is adjusting (adding or subtracting a clock pulse at) the 64 Hz clock. This signal can be selected by OUT2S as an output on the PSW. |
| 0x1D | B5 | CHGON | A value of 1 indicates that the CBC92141 is charging the backup battery. |
| 0x1D | B4 | OMODE | Oscillator mode. A value of 0 indicates that the RC oscillator is the source of the 256Hz system clock. A value of 1 indicates that the system clock is being derived from the XT oscillator. |
| 0x1D | B3 | SLEEP | This bit is set to 1 when SLP=1 and the pre-sleep timer reaches zero. A value of 1 indicates that the sleep controller is in the sleep state. This bit is automatically reset when an interrupt terminates the sleep state. Note: the Sleep Control Register 0x17 controls the behavior of I/O's in the sleep state, and some settings may disable the serial port. |
| 0x1D | B2 | IRQ | A value of 1 indicates an active interrupt as defined in the Interrupt Summary Table. |
| 0x1D | B1 | NIRQPIN | A value of 1 indicates that the CBC92141 is pulling the nPGD/NIRQ pin low. A value of 0 indicates that this pin is in an open-drain state. If the clock signal has been routed to this pin, then this status bit is not meaningful. |
| 0x1D | B0 | PGOOD | A value of 1 indicates VDD is valid and all I/O's are operational, including the serial ports. Exception: as long as VDD remains valid, the value of this bit remains 1 even when I/O's are disabled by the SLEEP controls. |

## Temperature ADC Registers 0x1E -0x1F (Read-Only)

| | | | |
|---|---|---|---|
| 0x1E | B7:B0 | Temp9-Temp2 | Temperature measurement results (MSB's). Top 8 bits from the 10-bit temperature ADC are reported here in Kelvin, where zero is absolute zero temperature (-273°C) and each count represents a 0.5°C step. |
| 0x1F | B7:B6 | Temp1-Temp0 | Temperature measurement results (LSB's). |
| 0x1F | B5:B0 | NOT USED | |

| | | | |
|---|---|---|---|
| 0x20-0x21 | B7:B0 | NOT USED | |

## Data Transfer Registers 0x22-0x23

| | | | |
|---|---|---|---|
| 0x22 | B7 | MEAS_TEMP | Toggling this bit from 0 to 1 updates the temperature reading stored in the TEMPADC and updates the temperature-compensated charging voltage based on the new temperature reading. When the new temperature readings are completed and stored in the TEMPADC registers, the CBC92141 will set the NEW_TEMP bit. The CBC92141 will not allow this bit to toggle to 1 when ADC_BUSY=1. |
| 0x22 | B6:B3 | NOT USED | |
| 0x22 | B2 | LATCH_CDT_OUT | A value of 1 causes the CBC92141 to wait for the second clock rising edge, then latch the current Countdown timer value into the CDT shadow register to be read by the serial port. This bit is automatically reset to zero when the CBC92141 sets LATCH_CDT_CMPLT to 1. |
| 0x22 | B1 | LOAD_DAT_IN | A value of 1 causes the CBC92141 to stop the RTC counters and synchronously (at 256 Hz) write time and calendar data (registers 0x00-0x07) from the serial –port accessible shadow registers to the respective RTC counter registers. Reset this value to zero to re-start the RTC time and date counters. |
| 0x22 | B0 | LATCH _OUT | A value of 1 causes the CBC92141 to wait for the second clock rising edge, then latch current RTC time and calendar counter data into the shadow registers to be read by the serial port. This bit is automatically reset to zero when the CBC92141 sets LATCH_ CMPLT to 1. |
| 0x23 | B7 | NEW_TEMP (Read/Clear-Only) | A value of 1 indicates that new temperature data requested by the MEAS_TEMP setting is available to be read over the serial port. This bit is automatically reset to zero when MEAS_TEMP is again set to 1 or when the internal charging controller initiates a temperature measurement |
| 0x23 | B6 | ADC_BUSY (Read-Only) | A value of 1 indicates that the charging controller is actively using the temperature measurement ADC. |
| 0x23 | B5:B3 | NOT USED | |
| 0x23 | B2 | LATCH_CDT_CMPLT | A value of 1 indicates that the data transfer from the Countdown Timer registers to the shadow register is complete and the data in 0x19 is ready to be read by the serial port. This bit is automatically reset to zero when it is read through the serial communications. |
| 0x23 | B1 | LOAD_ CMPLT (Read/Clear-Only) | A value of 1 indicates that the load of the new data from the shadow registers to the RTC counter registers is complete. This bit is automatically reset to zero when it is read through the serial communications and (if not previously reset) when LOAD_DAT_IN is again set to 1. |
| 0x23 | B0 | LATCH_ CMPLT (Read/Clear-Only) | A value of 1 indicates that the data transfer from the RTC counter registers to the shadow registers is complete and the data is ready to be read by the serial port. This bit is automatically reset to zero when it is read through the serial communications and (if not previously reset) when LATCH_ OUT is again set to 1. |

## Battery Management Configuration Registers 0x24

Note: The WBATMAN register must be set to 1 in order to allow updating of this register.

| | | | |
|---|---|---|---|
| 0x24 | B7:B4 | NOT USED | |
| 0x24 | B3 | VOUTEN | VOUT Enable. Set this to 1 to have backup battery supply available at the VOUT pin in backup mode. The VOUT switch (between the VOUT pin and the internal supply) is open in normal operation. A value of 0 will leave the switch open, even in backup mode. A value of zero reserves all available backup battery power exclusively to keep the real-time clock operating. WBATMAN must equal 1 to allow updating of this bit. |
| 0x24 | B2:B0 | BCMFREQ | Battery Cutoff Monitor Frequency. These 3 bits configure how frequently the CBC92141 checks the battery voltage in backup mode to see if it is below the cutoff threshold. The options for the monitoring intervals are provided in Table 9. The following application conditions would call for more frequent monitoring:<br>o lower capacity backup battery<br>o use of the XT oscillator in backup mode<br>o external loading at the VOUT pin<br>See the Electrical Characteristics table for the effect of battery monitoring and XT vs. RC oscillator on battery current draw. The battery monitoring operation draws power for a duration of less than or equal to 3 cycles of the 256 Hz clock.<br>If the battery voltage is found to be below the cutoff threshold, the cutoff switch will disconnect the battery at the CHG pin to protect it from damage. The WBATMAN value must equal 1 to allow updating of this value. |

**Table 9: Battery Cutoff Monitoring Frequency Interval (seconds) for settings of BCMFREQ register bits**

| 0x24 B2 | 0x24 B1 | 0x24 B0 | Hex value of 0x24 B3:B0 | Battery Cutoff Monitoring Frequency Interval (seconds on RTC count) |
|---|---|---|---|---|
| 0 | 0 | 0 | x0 | Continuous Monitoring |
| 0 | 0 | 1 | x1 | 1/8 |
| 0 | 1 | 0 | x2 | 1 |
| 0 | 1 | 1 | x3 | 4 |
| 1 | 0 | 0 | x4 | 8 |
| **1** | **0** | **1** | **x5 *** | **16** |
| 1 | 1 | 0 | x6 | 60 |
| 1 | 1 | 1 | x7 | 960 |

*** Default value is in bold**

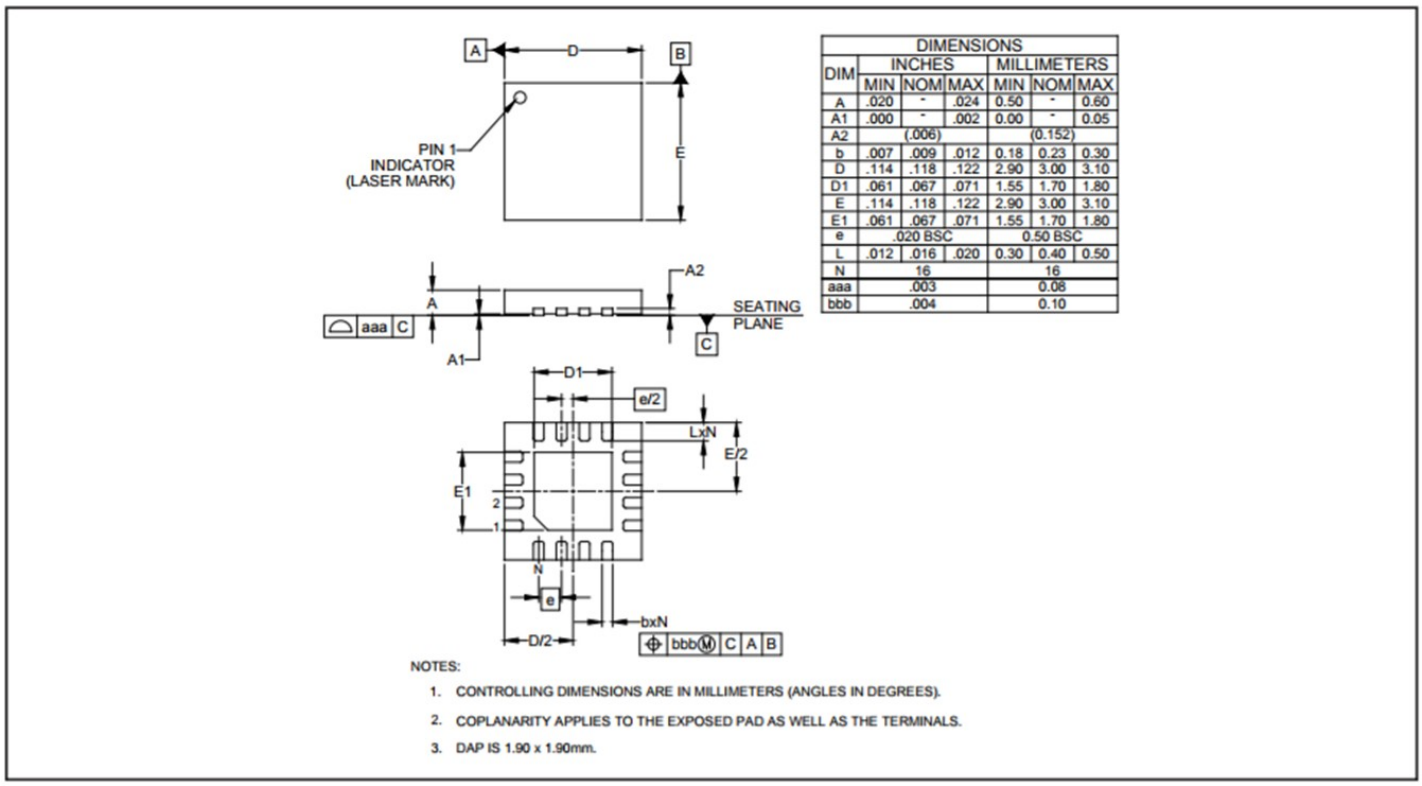
# Appendix: Charging Duty Cycle Tables

**Table 10:Charging duty cycles for charge frequency configurations and errors relative to target duty cycles**

| Charging duty cycle target vs. temperature | | | |
|---|---|---|---|
| -40°C to -20°C | -20°C to 0°C | 0°C to 40°C | 40°C to 85°C |
| 33% | 17% | 4% | 1% |

| Hex Code of B7:B4 | Charging Frequency vs. Temperature | | Charging Duty Cycle vs. Temperature | | | | Charging Duty Cycle Error Relative to Target | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | -40°C to +40°C | 40°C to 85°C | -40°C to -20°C | -20°C to 0°C | 0°C to 40°C | 40°C to 85°C | -40°C to -20°C | -20°C to 0°C | 0°C to 40°C | 40°C to 85°C |
| 0 | 32 days | 32 days | 25% | 12.5% | 3.1% | 1.0% | -25% | -25% | -25% | 0% |
| 1 | 32 days | 8 days | 25% | 12.5% | 3.1% | 1.0% | -25% | -25% | -25% | 0% |
| 2 | 32 days | 4 days | 25% | 12.5% | 3.1% | 1.0% | -25% | -25% | -25% | 0% |
| 3 | 32 days | 2 days | 25% | 12.5% | 3.1% | 0.7% | -25% | -25% | -25% | -33% |
| 4 | 8 days | 8 days | 25% | 12.5% | 4.2% | 1.0% | -25% | -25% | 0% | 0% |
| 5 | 8 days | 4 days | 25% | 12.5% | 4.2% | 1.0% | -25% | -25% | 0% | 0% |
| 6 | 8 days | 2 days | 25% | 12.5% | 4.2% | 0.7% | -25% | -25% | 0% | -33% |
| 7 | 8 days | 1 day | 25% | 12.5% | 4.2% | 1.4% | -25% | -25% | 0% | 33% |
| 8 | 4 days | 4 days | 25% | 25.0% | 4.2% | 1.0% | -25% | 50% | 0% | 0% |
| 9 | 4 days | 2 days | 25% | 25.0% | 4.2% | 0.7% | -25% | 50% | 0% | -33% |
| A | 4 days | 1 day | 25% | 25.0% | 4.2% | 1.4% | -25% | 50% | 0% | 33% |
| B | 4 days | 8 hours | 25% | 25.0% | 4.2% | 0.8% | -25% | 50% | 0% | -20% |
| C | 2 days | 2 days | 50% | 16.7% | 4.2% | 0.7% | 50% | 0% | 0% | -33% |
| D | 2 days | 1 day | 50% | 16.7% | 4.2% | 1.4% | 50% | 0% | 0% | 33% |
| E | 2 days | 8 hours | 50% | 16.7% | 4.2% | 0.8% | 50% | 0% | 0% | -20% |
| F | 1 day | 4 hours | 33% | 16.7% | 4.2% | 1.7% | 0% | 0% | 0% | 60% |

# Outline Drawing - 3x3 MLPQ-UT16

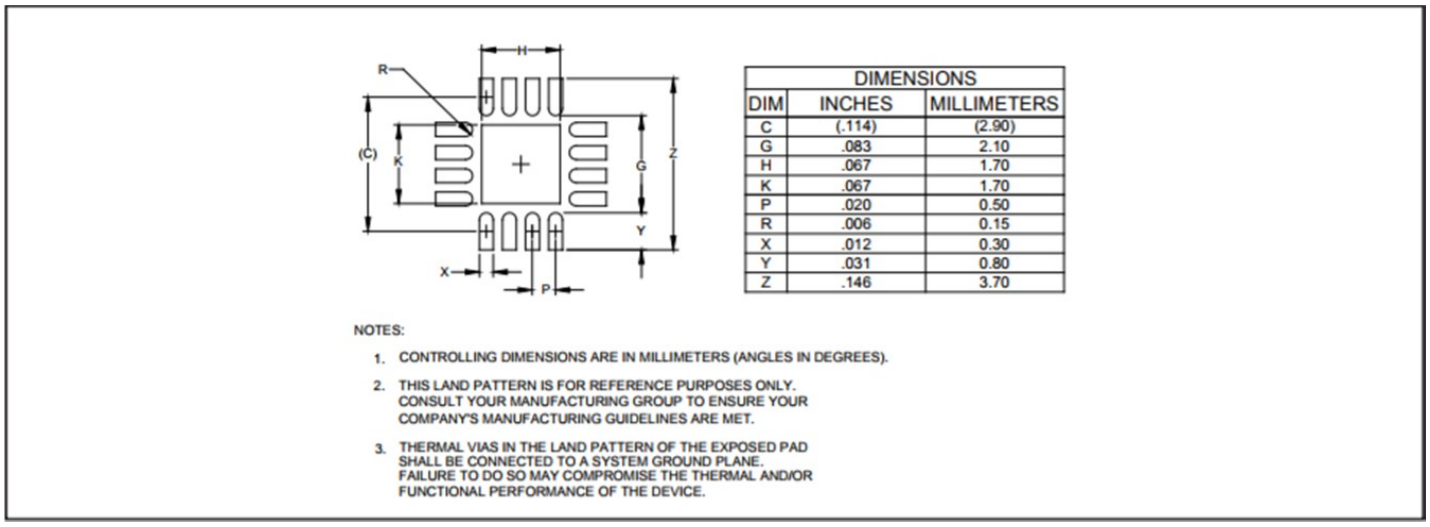



| DIM | DIMENSIONS | | | | | |
|---|---|---|---|---|---|---|
| | INCHES | | | MILLIMETERS | | |
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | .020 | - | .024 | 0.50 | - | 0.60 |
| A1 | .000 | - | .002 | 0.00 | - | 0.05 |
| A2 | | (.006) | | | (0.152) | |
| b | .007 | .009 | .012 | 0.18 | 0.23 | 0.30 |
| D | .114 | .118 | .122 | 2.90 | 3.00 | 3.10 |
| D1 | .061 | .067 | .071 | 1.55 | 1.70 | 1.80 |
| E | .114 | .118 | .122 | 2.90 | 3.00 | 3.10 |
| E1 | .061 | .067 | .071 | 1.55 | 1.70 | 1.80 |
| e | .020 BSC | | | 0.50 BSC | | |
| L | .012 | .016 | .020 | 0.30 | 0.40 | 0.50 |
| N | 16 | | | 16 | | |
| aaa | .003 | | | 0.08 | | |
| bbb | .004 | | | 0.10 | | |

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
3. DAP IS 1.90 x 1.90mm.

# Land Pattern - 3x3 MLPQ-UT16




| DIMENSIONS | | |
|---|---|---|
| DIM | INCHES | MILLIMETERS |
| C | (.114) | (2.90) |
| G | .083 | 2.10 |
| H | .067 | 1.70 |
| K | .067 | 1.70 |
| P | .020 | 0.50 |
| R | .006 | 0.15 |
| X | .012 | 0.30 |
| Y | .031 | 0.80 |
| Z | .146 | 3.70 |

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

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