< GSGL-0003 >

GNSS SiP Module

Pb-free, halogen-free and RoHS compliant

Restricted

1. Security warning

2. Publication history

Revision History		Product name	GSGL-0003 Module	
		Part No.	GSGL-0003	
Version	Date	Contents of change	Author	Remarks
V0.1	2021/12/28	First Edition	Cesar.Wang	
V0.2	2022/05/18	Update RF Characteristics	Vivi.Cui	
V0.3	2022/05/25	Update RF Characteristics Update Current Consumption	Vivi.Cui	

Content

1. Introduction

1.1 Functional Description

GSGL-0003 module is based on System in Package (SiP) technology which consists of a Sony CXD5609AGF GNSS, an Infineon BGA123N6 LNA, a Qualcomm SAW filter, a Gigadevice Flash and the matched passive components. All components are integrated in a tiny 47 pins 5.3x4.9x0.94 mm^3 LGA package with sputter technology to achieve EMI shielding. GSGL-0003 can be used to scheme location application for consumer electronics.

The CXD5609AGF is a multi-GNSS receiver with a nor sensitivity and fast acquisition engine. It can operate from a single supply rail from 0.7V to 1.8V. Meanwhile, it supports GLONASS, SBAS, QZSS, BeiDou and Galileo location with low power consumption. Besides, it is compatible with both UART and I2C interface to transmit location data.

The BGA123N6 is designed to enhance GNSS signal sensitivity and operate in a wide supply voltage range of 1.1V to 3.3V with ultra low current consumption of 1.3mA. What's more. It is used in the frequency of 1550 to 1615 MHz with insertion power gain of 19dB and low noise figure of 0.75 dB.

The B38162W1203W310 is a RF single filter for BeiDou, GPS and GLONASS with the min attenuation of 25dB. It has excellent insertion attenuation of 0.8 dB with center frequency of 1582.47MHz.

An 8 Mbit serial Flash, GD25LE80E is connected to the GNSS through SPI, because the internal MRAM of CXD5609AGF is incompatible with the temperature and pressure applied during the molding process.

1.2 Features

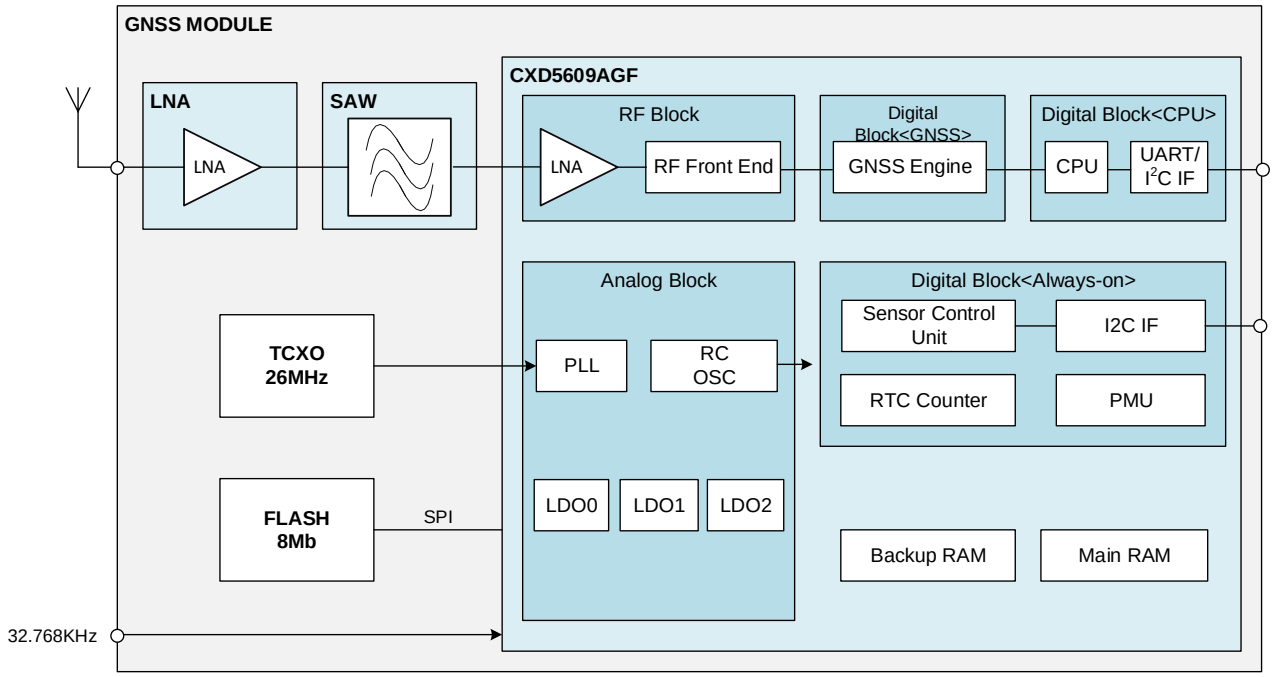
CXD5609AGF Receiver

- A multi-GNSS module for GPS, GLONASS, SBAS, QZSS, BeiDou and Galileo
- Ultra-low power consumption
- Embedded noise filters and spectrum analyzer for development
- 1.8V Host MCU interface IO of UART and I2C

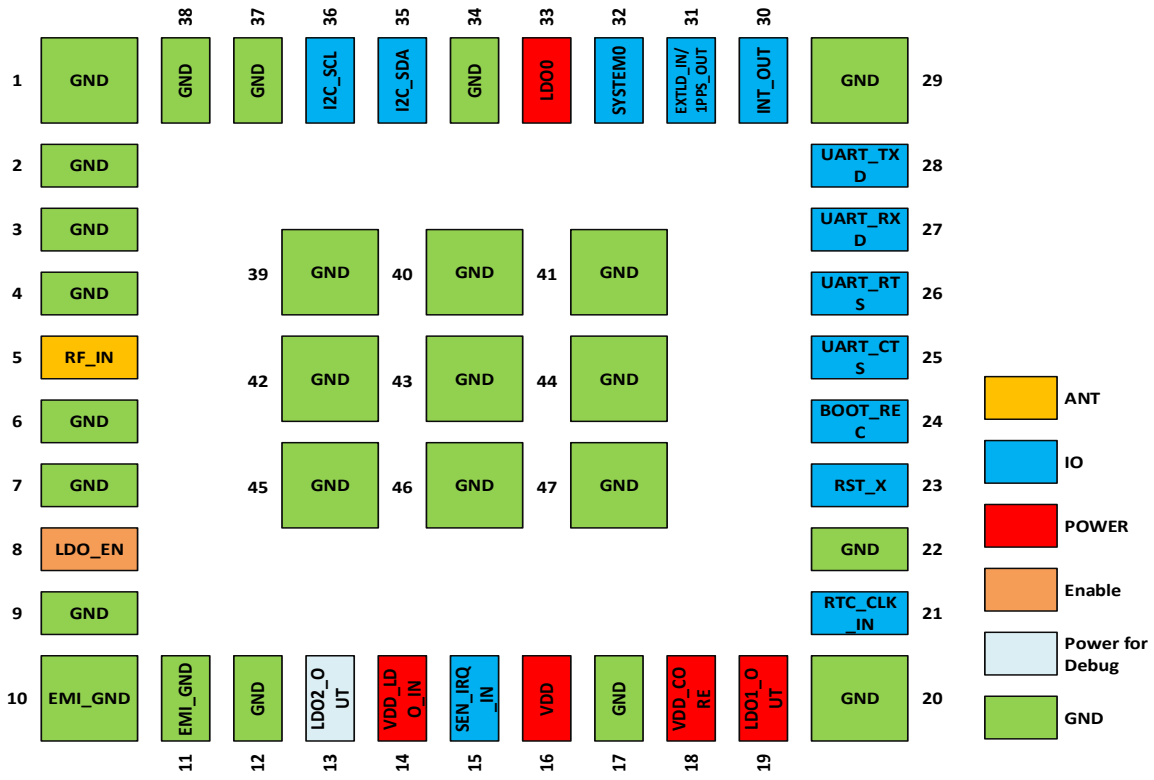
GSGL-0003 module

- Featuring integrated GNSS
- Low power consumption
- Small size of 5.3x4.9x0.94 mm^3 suitable for low volume system integration
- Easy for integration into mobile and handheld device with flexible system configuration

2. Block Diagram



3. Pin Map and Description



Top view

Pin#	Pin Name	Type	IO Power Supply	Reset State	Description
1	GND	P	/	/	Ground
2	GND	P	/	/	Ground
3	GND	P	/	/	Ground
4	GND	P	/	/	Ground
5	RF_IN	I	VDD_IO_ANA	/	GNSS RF Signal Input
6	GND	P	/	/	Ground
7	GND	P	/	/	Ground
8	LDO_EN	I	VDD_IO_ANA	/	LDO0/LDO1 Enable
9	GND	P	/	/	Ground
10	GND	P	/	/	Ground
11	GND	P	/	/	Ground
12	GND	P	/	/	Ground
13	LDO2_OUT	P	VDD_IO_ANA	/	LDO Output for Memory Block
14	VDD_LDO_IN	P	VDD_IO_ANA	/	LDO0/LDO1 Input
15	SEN_IRQ_IN	I/O	VDD_IO1	Hi-Z	Interrupt Input
16	VDD	P	/	/	Power In
17	GND	P	/	/	Ground
18	VDD_CORE	P	/	/	Digital Block Power
19	LDO1_OUT	P	VDD_IO_ANA	/	LDO Output for Digital Blocks
20	GND	P	/	/	Ground
21	RTC_CLK_IN	I	VDD_IO1	Hi-Z	RTC Clock Input
22	GND	P	/	/	Ground
23	RST_IN	I	VDD_IO1	Hi-Z	Reset Input
24	BOOT_REC	I/O	VDD_IO1	Pull-down	Boot Recovery
25	UART_CTS	I/O	VDD_IO0	Hi-Z	UART_CTS
26	UART_RTS	I/O	VDD_IO0	Hi-Z	UART_RTS
27	UART_RXD	I/O	VDD_IO0	Hi-Z	UART_RXD/I2C SDA
28	UART_TXD	I/O	VDD_IO0	Hi-Z	UART_TXD/I2C SCL
29	GND	P	/	/	Ground
30	INT_OUT	I/O	VDD_IO0	Hi-Z	Interrupt Output/ 1PPS Out

31	EXTLD_IN/1PPS_OUT	I/O	VDD_IO0	/	Timing input/1PPS Out
32	SYSTEM0	I	VDD_IO1	Hi-Z	Boot Mode
33	LDO0	P	/	/	LDO Output for Analog Blocks
34	GND	P	/	/	Ground
35	I2C_SDA	I/O	VDD_IO1	Hi-Z	I2C SDA
36	I2C_SCL	I/O	VDD_IO1	Hi-Z	I2C SCL
37	GND	P	/	/	Ground
38	GND	P	/	/	Ground
39	GND	P	/	/	Ground
40	GND	P	/	/	Ground
41	GND	P	/	/	Ground
42	GND	P	/	/	Ground
43	GND	P	/	/	Ground
44	GND	P	/	/	Ground
45	GND	P	/	/	Ground
46	GND	P	/	/	Ground
47	GND	P	/	/	Ground

Note: LDO1_OUT should be open if not used.

4. Electrical Characteristics

4.1 Absolute Maximum Ratings

Parameter		Min	Max	Unit
Supply Power	VDD	-0.3	2.5	V
	VDD_LDO_IN	-0.3	VDD+0.3	V
	LDO0&VDD_CORE	-0.3	1.4	V
Operating Temperature		-30	85	°C
Storage Temperature		-40	85	°C

4.2 Recommended Operation Conditions

Parameter		Min	Type	Max	Unit
Supply Power	VDD	1.71	1.80	1.89	V
	VDD_LDO_IN	0.90	/	1.95	V
	LDO0&VDD_CORE	0.65	0.70	0.75	V

Note: VDD_LDO_IN must be this input voltage level even if the LDOs are not used.

4.3 Digital IO Characteristics

Item	Symbol	Min	Max	Unit
Input Voltage	V_{IH}	0.7x IO Supply Voltage	IO Supply Voltage+0.3	V
	V_{IL}	-0.3	0.3x IO Supply Voltage	V
Output Voltage	V_{OH}	0.8x IO Supply Voltage	/	V
	V_{OL}	/	0.2x IO Supply Voltage	V
Drivability (VDD_IO0)	I_{OH}	1.2	/	mA
	I_{OL}	1.2	/	mA
Drivability (VDD_IO1)	I_{OH}	2	/	mA
	I_{OL}	2	/	mA

4.4 Current Consumption

Embedded LDO supply (Typical spec is defined as VDD_LDO_IN @1.8V at 25℃)

Item	State	Typ	Max	Unit
Satellite Acquisition@Cold Start	S0: Exec	15	-	mA
Satellite Tracking		11	-	mA
Idle@Waiting for Command	S1: Idle	2	-	mA
Sleep0	S2: Sleep0	400	-	uA
Sleep1	S3: Sleep1	64	-	μA

Embedded LDO supply (Typical spec is defined as VDD @1.8V at 25℃)

Item	State	Typ	Max	Unit
Satellite Acquisition@Cold Start	S0: Exec	3	-	mA
Satellite Tracking		3	-	mA
Idle@Waiting for Command	S1: Idle	1.6	-	mA
Sleep0	S2: Sleep0	200	-	uA
Sleep1	S3: Sleep1	120	-	μA
boot-up internal LDOs use	-	-	300	mA

Note: This current flows for 10 ms (ave) to 30 ms (max) at boot-up time when power for the VDD_CORE is supplied from LDO1.

External power supply (Typical spec is defined as VDD_CORE @0.7V at 25℃)

Item	State	Typ	Max	Unit
Satellite Acquisition@Cold Start	S0: Exec	12	-	mA
Satellite Tracking		8	-	mA
Idle@Waiting for Command	S1: Idle	1.8	-	mA
Sleep0	S2: Sleep0	250	-	uA
Sleep1	S3: Sleep1	30	-	μA

External power supply (Typical spec is defined as VDD @1.8V at 25℃)

Item	State	Typ	Max	Unit
Satellite Acquisition@Cold Start	S0: Exec	3	-	mA
Satellite Tracking		3	-	mA
Idle@Waiting for Command	S1: Idle	1.6	-	mA
Sleep0	S2: Sleep0	170	-	uA
Sleep1	S3: Sleep1	70	-	μA

External power supply (Typical spec is defined as LDO0 @0.7V at 25℃)

Item	State	Typ	Max	Unit
Satellite Acquisition@Cold Start	S0: Exec	2.3	-	mA
Satellite Tracking		2.3	-	mA
Idle@Waiting for Command	S1: Idle	120	-	uA
Sleep0	S2: Sleep0	13	-	uA
Sleep1	S3: Sleep1	13	-	μA

5. RF Characteristics

5.1 GNSS Receiver Performance Specifications

The GSGL-0003 module complies with the following features and standards.

Items	Description
Satellite Systems	GPS, GLONASS, QZSS, SBAS, BeiDou, Galileo
Frequency Band	GPS L1, C/A
	GLONASS L1,OF
	QZSS L1 C/A
	SBAS L1,C/A
	BeiDou B1
	Galileo E1,CBOC

5.2 Position Accuracy

Item	GPS	GPS&GLONASS	Unit	Remarks
2DRMS	1	1	m	Signal Power is -130dBm

5.3 Time-To-First-Fix(TTFF)

Item	GPS	GPS&GLONASS	Unit	Remarks
Cold Start	<35	<35	s	Signal Power is -130dBm
Hot Start	<2	<2	s	

5.4 Sensitivity

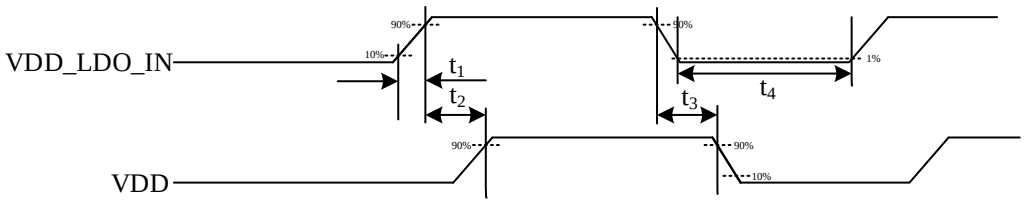
Item	GPS	GPS&GLONASS	Unit	Remarks
Cold Start	-148	-148	dBm	
Hot Start	-161	-161	dBm	
Tracking	-162	-162	dBm	

5.5 RF Performance

Item	Specification	Unit	Remark
Noise Figure	<1	dB	

6. Sequence and Timing

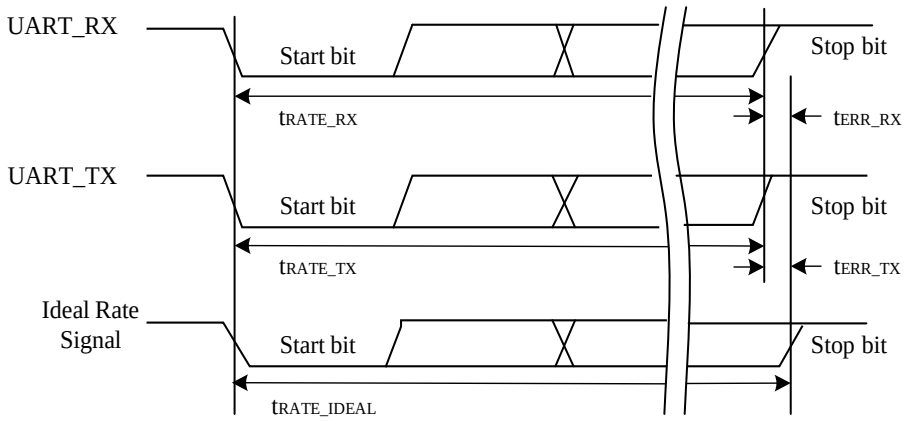
6.1 Power-on



Embedded LDO supply:

Item	Symbol	Min	Max	Unit
VDD_LDO_IN rise time	t_1	0.08	4	ms
Time Difference from VDD_LDO_IN rise to VDD rise	t_2	-1	5	ms
Time Difference from VDD_LDO_IN fall to VDD fall	t_3	-10	0	ms
Power off period	t_4	100	/	ms

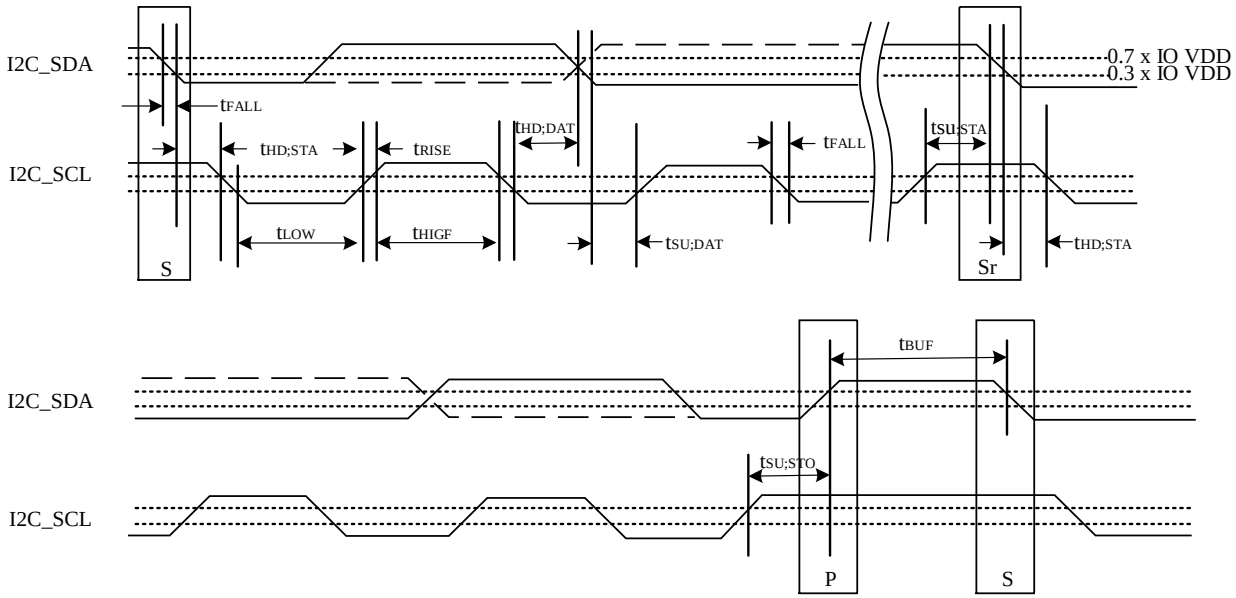
6.2 UART



Item	Symbol	Min	Typ	Max	Unit	Remarks
UART Error Rate (except TX@115.2kbps)	R_{BRT_ERR}	-1	—	1	%	t_{ERR_TX} / t_{RATE_IDEAL} t_{ERR_RX} / t_{RATE_IDEAL}
UART Error Rate (TX@115.2kbps)	$R_{BRT\_ERR\_FD\_TX}$	-4	—	4	%	t_{ERR_TX} / t_{RATE_IDEAL}

These timing budgets are changed by PCB (Printed Circuit Board) design. Please evaluate UART function on your PCB carefully.

6.3 I2C(Host interface and Slave interface)



Item	Symbol	Standard-Mode		Fast-Mode		FAST-Mode Plus		Unit	Remarks
		Min	Max	Min	Max	Min	Max		
SCL clock frequency	f_{SCl}	0	100	0	400	0	1000	KHz	—
HOLD time(repeated). START condition	$t_{HD;STA}$	4	—	0.6	—	0.26	—	μs	—
LOW period of the SCL clock	t_{LOW}	4.7	—	1.3	—	0.5	—	μs	—
LOW period of the SCL clock	t_{HIGH}	4	—	0.6	—	0.26	—	μs	—
Setup time for a repeated START condition	$t_{SU;STA}$	4.7	—	0.6	—	0.26	—	μs	—
Data hold time	$t_{HD;DAT}$	0	—	0	—	—	—	μs	—
Data setup time	$t_{SU;DAT}$	250	—	100	—	50	—	ns	—
Rise time of both SDA and SCL signals	t_{RISE}	—	1000	20	300	—	120	ns	—
Fall time of both SDA and SCL signals	t_{FALL}	—	300	—	300	—	120	ns	—
Setup time for STOP condition	$t_{SU;STO}$	4	—	0.6	—	0.26	—	μs	—

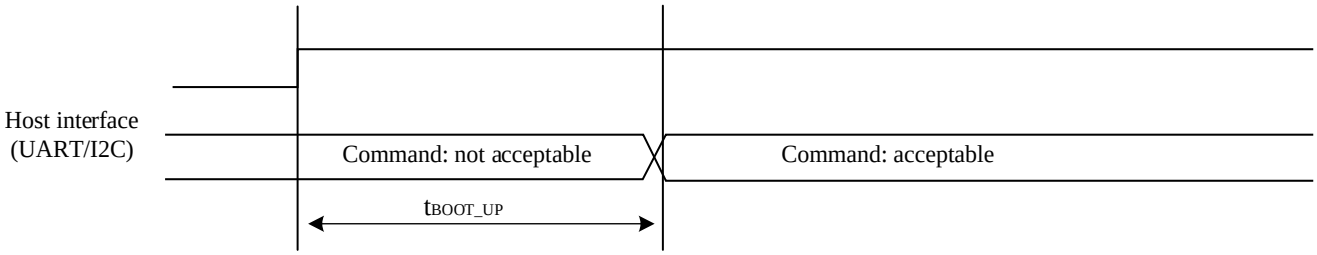
Bus free time between STOP and START condition	t_{BUF}	4.7	—	1.3	—	0.5	—	μs	—
Capacitive load for each bus line	C_L	—	73	—	73	—	29	pF	4.7KΩ Pull-up

6.4 Others

RTC_CLK_IN

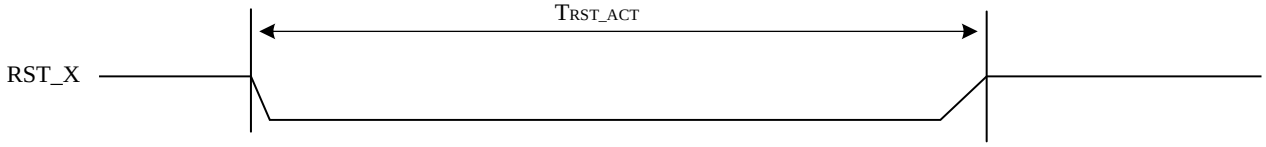
Item	Symbol	Min	Typ	Max	Unit
Input Frequency	F_{IN}	—	32.768	—	KHz
Frequency Tolerance	F_{IN_T}	-300	—	300	ppm
Duty Cycle	D_C	5	—	95	%

Boot-up



Item	Symbol	Min	Typ	Max	Unit	Remarks
Time to accept commands from the system reset asserting	t_{BOOT_UP}	—	—	1000	ms	Boot-up with the recommended external FLASH memory

Reset



Item	Symbol	Min	Typ	Max	Unit	Remarks
RST assert period	t_{RST_ACT}	100	—	—	ms	—

Note：the pin has connected to pull up resistor of 100kΩ in the module.

Host MCU interface

The following are provided as interfaces to the host MCU.

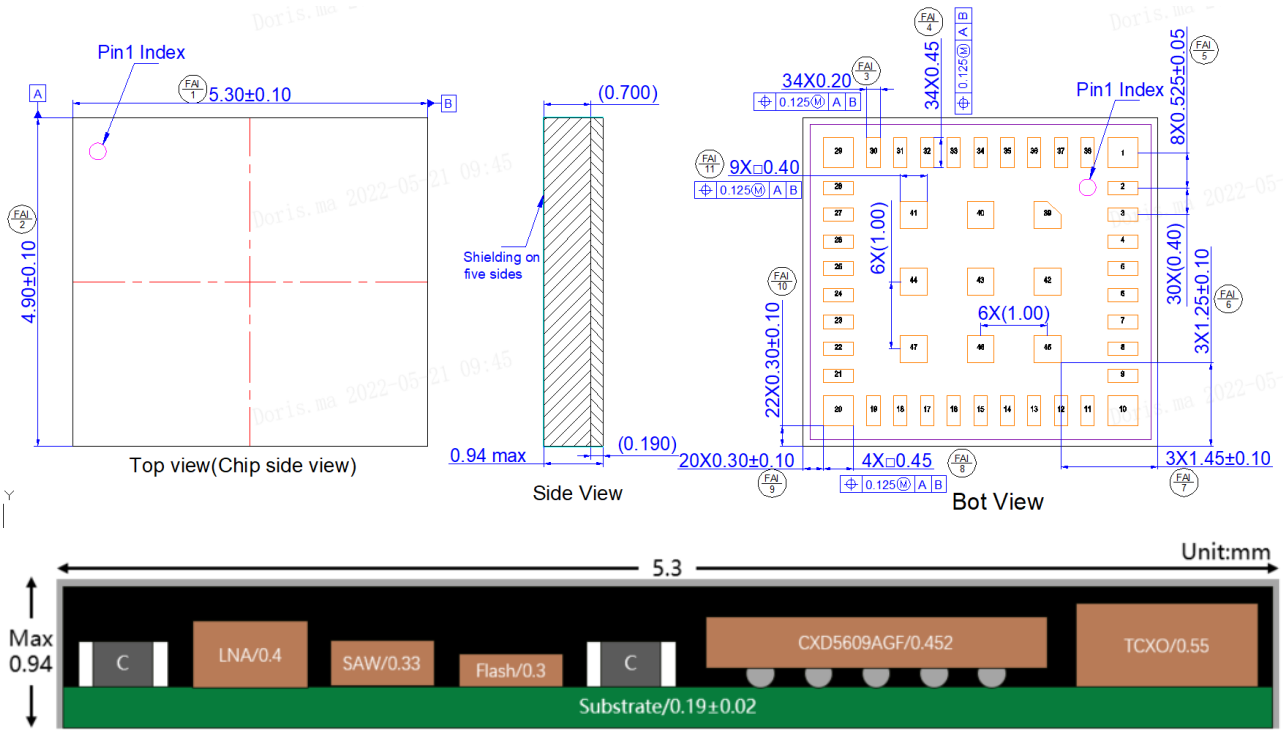
- UART: up to 1.00 Mbps (8-N-1), up to 2.00 Mbps (8-N-2).
- I2C: Standard mode (100 Kbps), Fast mode (400 Kbps) and Fast mode plus (1 Mbps).

The interface selection is set by the SYSTEM0 pins.

SYSTEM0	Selected interface
0	I2C
1	UART

7.Physical Specifications

7.1 Package Outline



7.2 Laser Marking Drawing

TBD

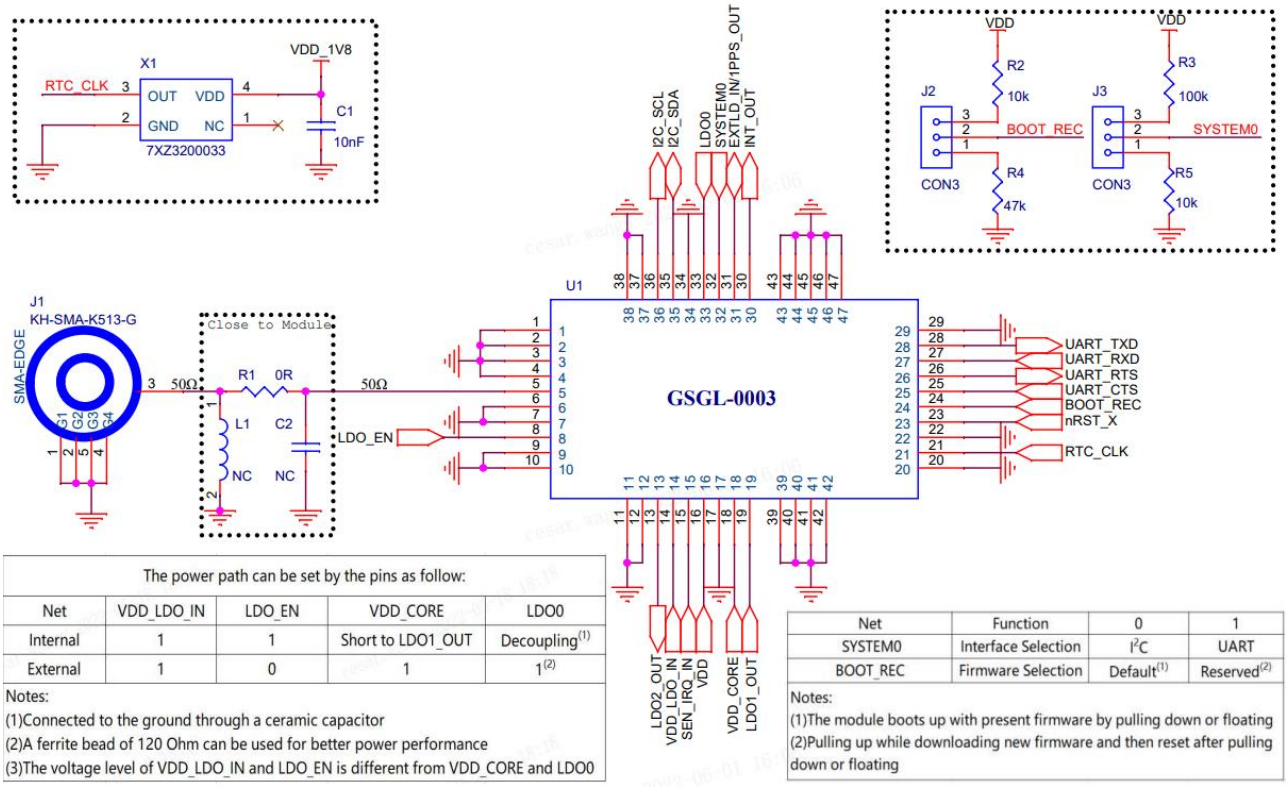
7.3 Recommendation Reflow Profile

TBD

7.4 Package and Storage Condition

TBD

8. Reference Application Circuit



The power path can be set by the pins as follow:				
Net	VDD_LDO_IN	LDO_EN	VDD_CORE	LDO0
Internal	1	1	Short to LDO1_OUT	Decoupling(1)
External	1	0	1	1(2)

Notes:
(1)Connected to the ground through a ceramic capacitor
(2)A ferrite bead of 120 Ohm can be used for better power performance
(3)The voltage level of VDD_LDO_IN and LDO_EN is different from VDD_CORE and LDO0

Net	Function	0	1
SYSTEM0	Interface Selection	I²C	UART
BOOT_REC	Firmware Selection	Default(1)	Reserved(2)

Notes:
(1)The module boots up with present firmware by pulling down or floating
(2)Pulling up while downloading new firmware and then reset after pulling down or floating