
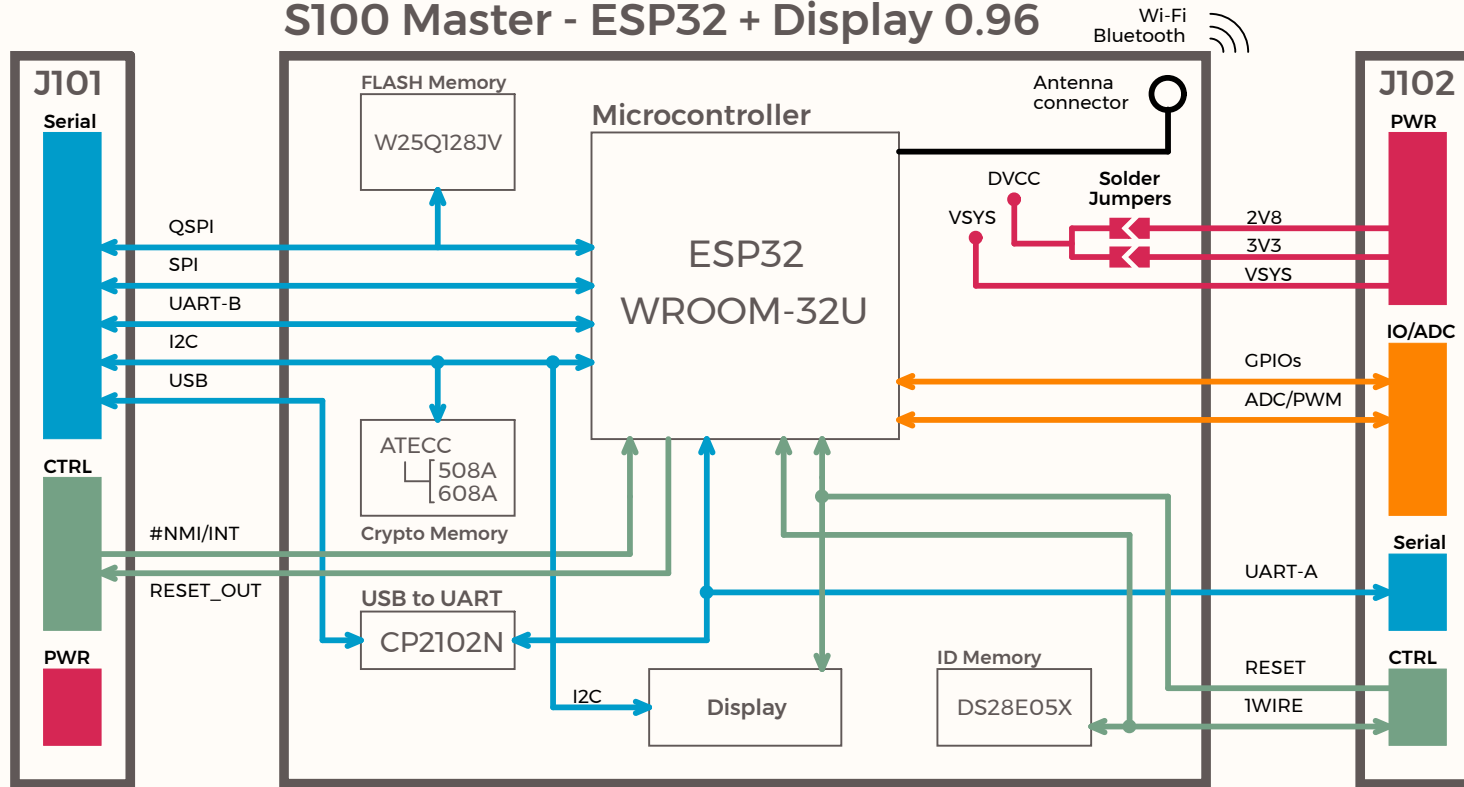


S100 Master - ESP32 + Display 0.96

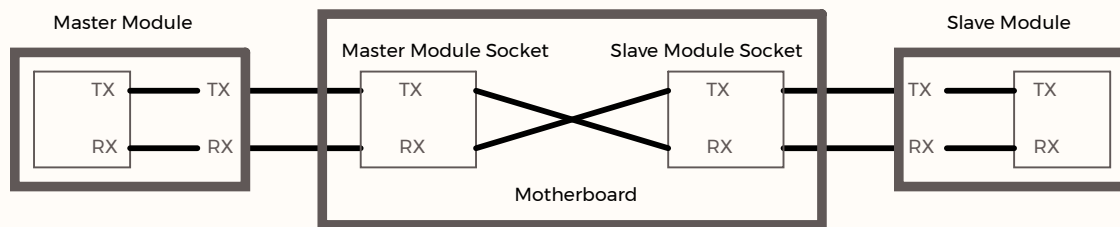
Page	Title
1	Index
2	Block Diagram
3	S100 Master - Plug
4	ESP32-WROOM-32U
5	Display 0.96 & Memories
6	Production

Title: 01. Index.SchDoc		 rhombio Free to Create
Engineer: D.A.M. & G.A.M.	Date: 04/02/2019	
Project: S100 Master - ESP32 + Display 0.96.PrjPcb		
Revision: v1.0	Sheet: 1 of 6	

S100 Master - ESP32 + Display 0.96



UART CONNECTIONS

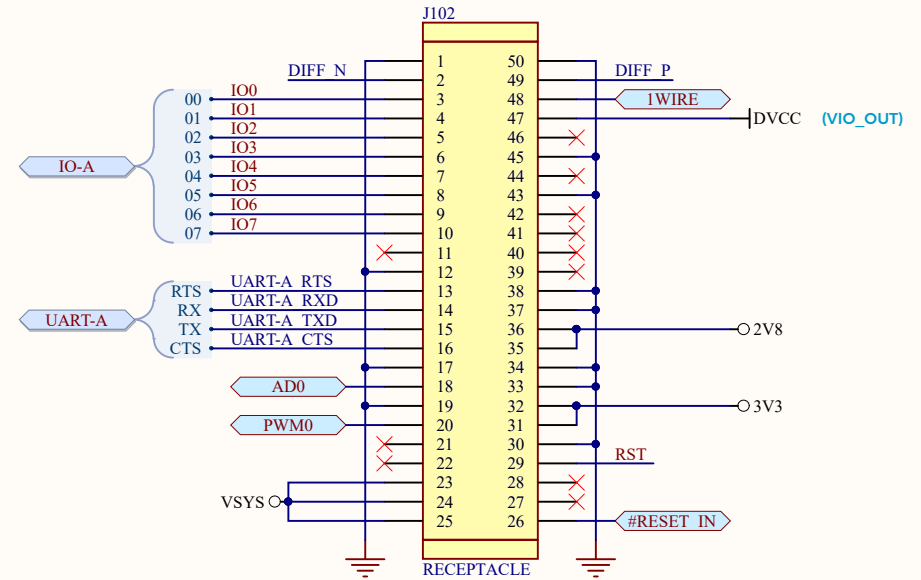
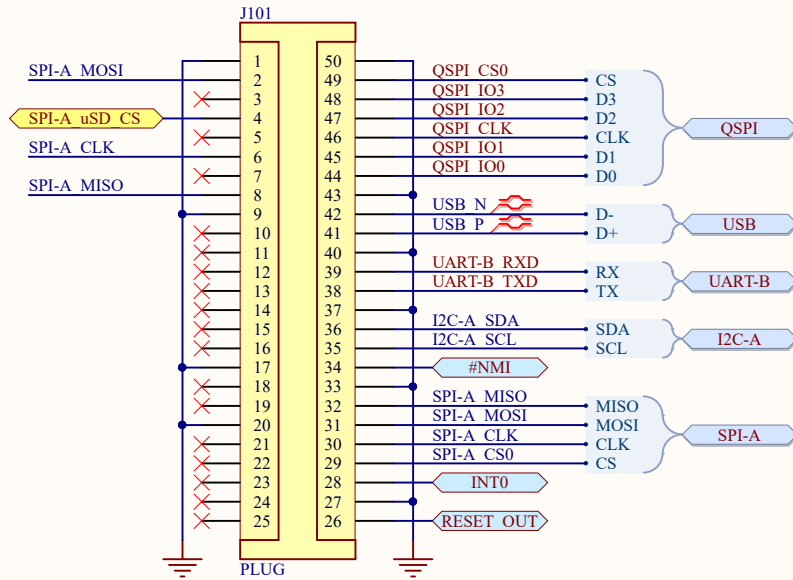


Title: 02. Block Diagram.SchDoc	
Engineer: D.A.M. & G.A.M.	Date: 04/02/2019
Project: S100 Master - ESP32 + Display 0.96.PrjPcb	
Revision: v1.0	Sheet: 2 of 6



S100 MASTER - PLUG

Transparent TOP VIEW



~~#RESET IN~~ ~~RST~~

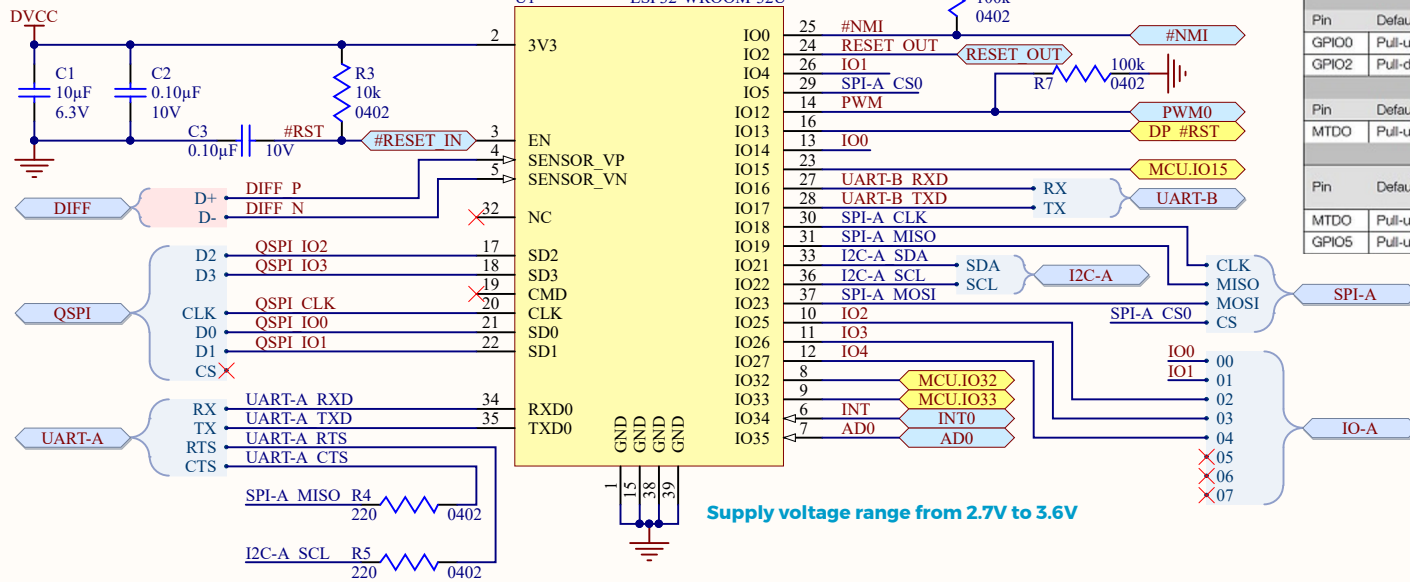
DESIGN NOTE:

- I2C pull-up resistors are placed on the motherboard, not on the module.
- UART, CAN & SAI lines are crossed on the motherboard, not on the module.
- The text of the unused nets have been deleted.

Title: 03. S100 Master - Plug.SchDoc	
Engineer: D.A.M. & G.A.M.	Date: 04/02/2019
Project: S100 Master - ESP32 + Display 0.96.PrjPcb	
Revision: v1.0	Sheet: 3 of 6

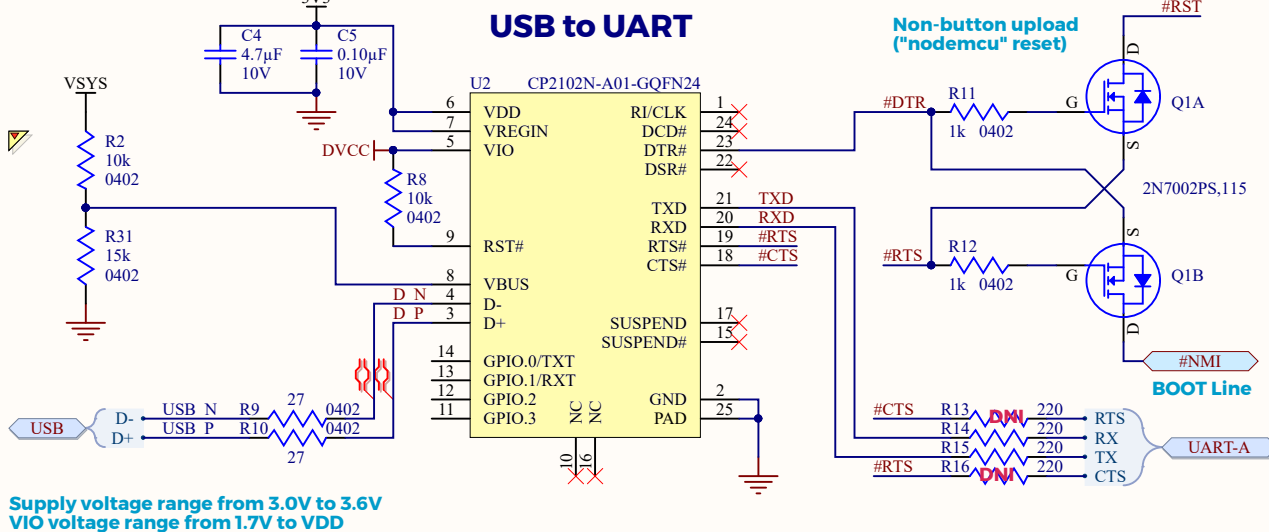


ESP32-WROOM-32U



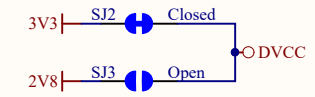
		Voltage of Internal LDO (VDD_SDIO)			
Pin	Default	3.3V	1.8V		
MTDI	Pull-down	0	1		
Booting Mode					
		SPI Boot	Download Boot		
GPIO0	Pull-up	1	0		
GPIO2	Pull-down	Don't-care	0		
Enabling/Disabling Debugging Log Print over U0TXD During Booting					
		U0TXD Active	U0TXD Silent		
MTDO	Pull-up	1	0		
Timing of SDIO Slave					
Pin	Default	Falling-edge Input	Rising-edge Input	Falling-edge Output	Rising-edge Output
MTDO	Pull-up	0	0	1	1
GPIO5	Pull-up	0	1	0	1

NMI line is usually pulled-up at motherboards and tied to a button

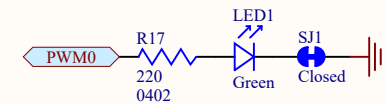


Non-button upload ("nodemcu" reset)

VOLTAGE SELECTOR



USER LED



Title: 04. ESP32-WROOM-32U.SchDoc

Engineer: D.A.M. & G.A.M. Date: 04/02/2019

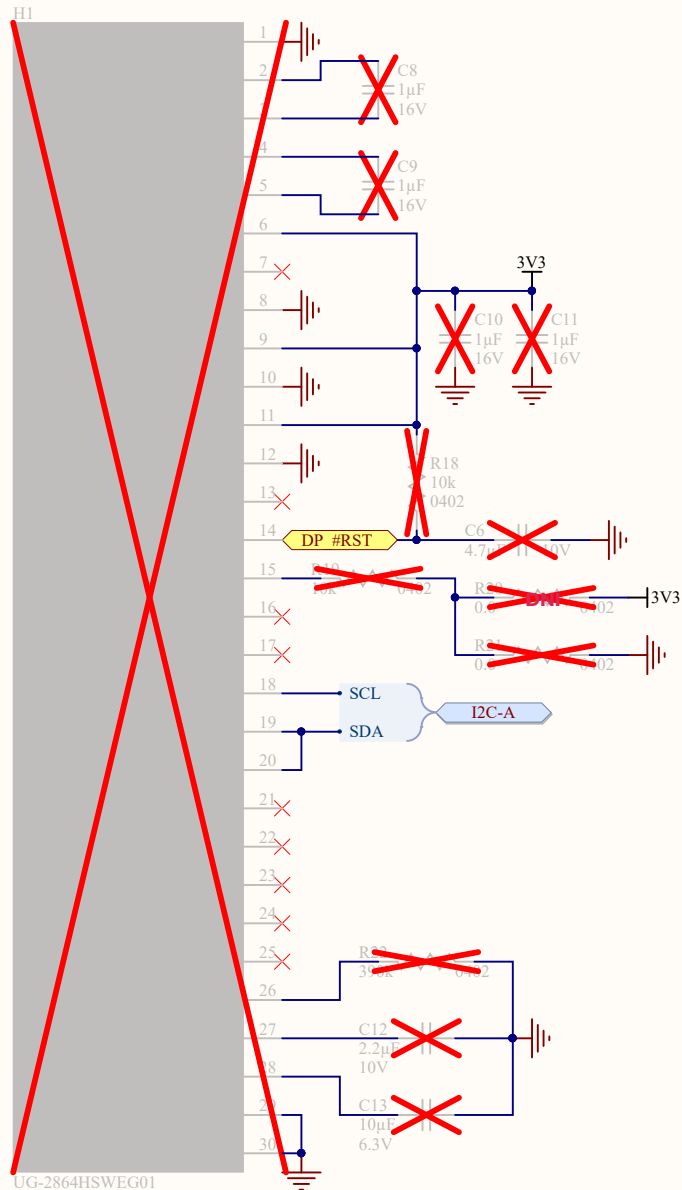
Project: S100 Master - ESP32 + Display 0.96.PrjPcb

Revision: v1.0

Sheet: 4 of 6

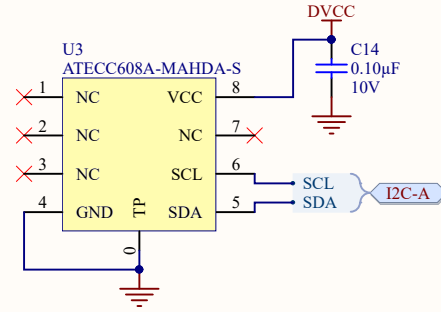


DISPLAY 0.96"



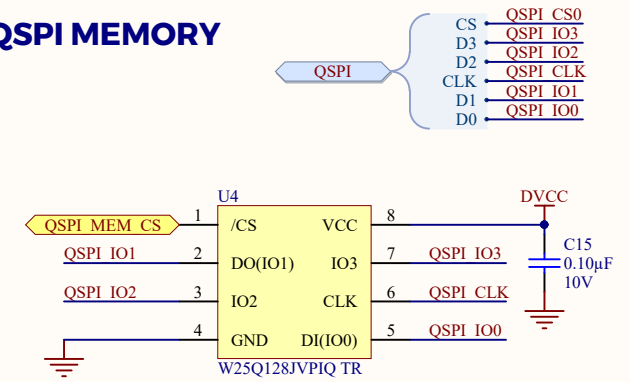
UG-2864HSWEG01

SECURITY

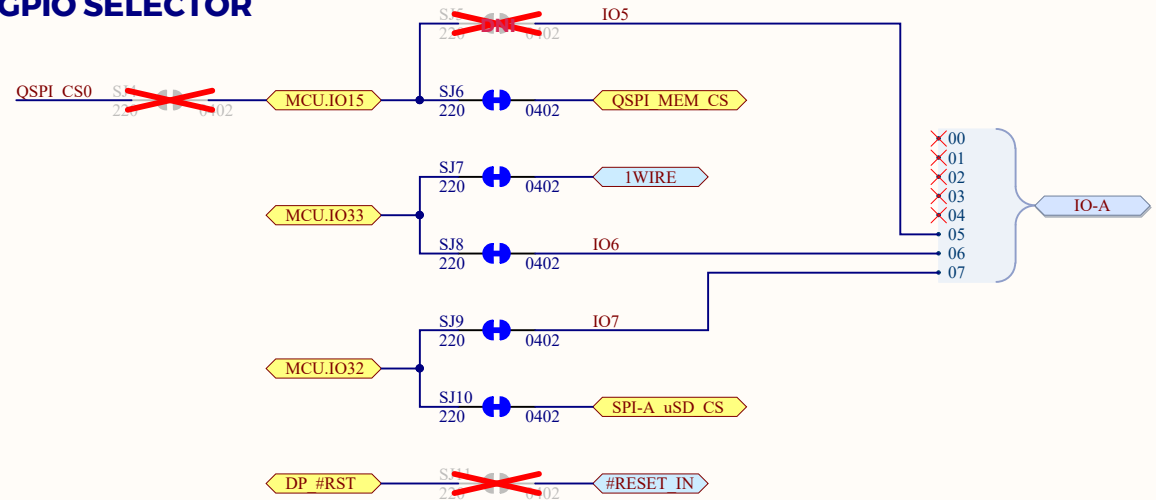


Supply voltage range from 2.0V to 5.5V

QSPI MEMORY



GPIO SELECTOR



Title: 05. Display 0.96 & Memories.SchDoc

Engineer: D.A.M. & G.A.M. Date: 04/02/2019

Project: S100 Master - ESP32 + Display 0.96.PrjPcb

Revision: v1.0

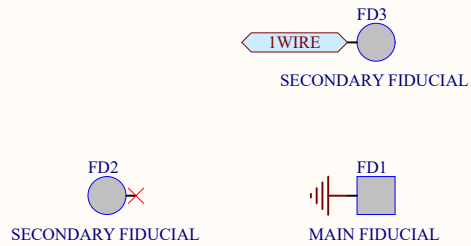
Sheet: 5 of 6



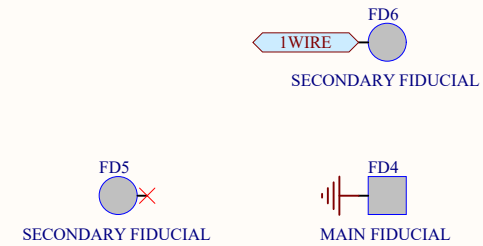
PCB

A PCB
S100 Master
ESP32 + Display 0.96
RLRHMESSP32D101809

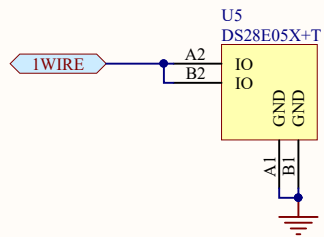
TOP LAYER FIDUCIALS



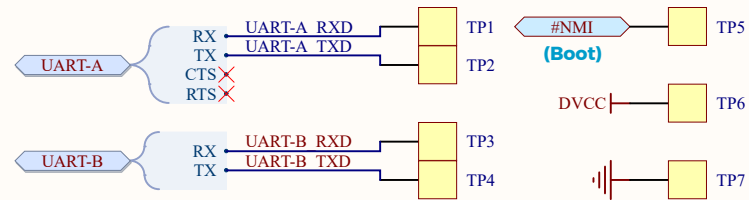
BOTTOM LAYER FIDUCIALS



ID EEPROM



TEST PADS



Title: 06. Production.SchDoc

Engineer: D.A.M. & G.A.M. Date: 04/02/2019

Project: S100 Master - ESP32 + Display 0.96.PrjPcb

Revision: v1.0

Sheet: 6 of 6

